UFSOI Model Parameter Evaluation: Process-Based Calibration

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1. Introduction

The UFSOI FD [1] and NFD [2] MOSFET models are physical and process-based, meaning that their key parameters relate directly to device structure and physics. The parameter evaluation thus can be and should be done based on knowledge of the SOI technology [3]. The model-calibration methodology should include some tuning of particular parameters based on electrical measurements of devices having more than one channel length and width in specific bias regions. The methodology can be defined with good physical insight to be reliable and much simpler than conventional parameter extraction, or optimization via least-squares fits to measured data. In fact, such a process-based methodology seems essential for reliable SOI model calibration because of complications due to device self-heating and dynamic floating-body effects [4].

This report, expanded beyond its previous (4.41) version dated March 1998, extends and refines the parameter-evaluation algorithm described in [3], yielding a straightforward calibration methodology for the UFSOI/Ver. 4.5 models [5] which requires minimal knowledge of device structure, measured DC current-voltage characteristics of two floating-body devices having long and short (target) channel lengths, and a measured gate capacitance-voltage characteristic. The systematic process-based methodology is amenable to implementation in software for automated parameter evaluation. (Its use in UTMOST [6] has been effected.) The methodology is demonstrated here via application to AMD's 0.35μm NFD/SOI CMOS technology [7] and to MIT Lincoln Lab's 0.25μm FD/SOI CMOS technology [8].

2. Parameter Evaluation for NFD/SOI MOSFETs

Unlike bulk-Si MOSFET models, SOI device models must be properly calibrated to account for both DC and dynamic floating-body effects. The charge-based UFSOI NFD model formalism is BiMOS [3], accounting for parasitic bipolar features, intrinsically coupled to the MOS analysis, which underlie these effects. The process-based nature of the model enables a quick preliminary parameter estimation based on device structure and physics, which facilitates the subsequent systematic and efficient tuning of a few key parameters via specific device measurements. The Ver. 4.5 model parameters, along with their descriptions and typical values for current state-of-the-art NFD/SOI technologies, are listed in Table 1 [5].

Table 1: UFSOI-4.5 NFD MOSFET Model Parameters

Name	Description	Units	Default	Typical Values
NQFF	Front oxide fixed charge (normalized)	cm^{-2}	0.0	$\sim 10^{10}$
NQFB	Back oxide fixed charge (normalized)	cm^{-2}	0.0	$\sim 10^{11}$
NQFSW	Effective sidewall fixed charge (0 for no narrow-width effect)	cm^{-2}	0.0	$\sim\pm 10^{12}$
TOXF	Front-gate oxide thickness	m	$10.x10^{-9}$	$(3\text{-}8)x10^{-9}$
TOXB	Back-gate oxide thickness	m	$500.x10^{-9}$	$(80\text{-}400)x10^{-9}$
NSUB	Substrate doping density	cm^{-3}	$1.0x10^{15}$	$10^{15}\text{-}10^{17}$
NGATE	Poly-gate doping density (0 for no poly-gate depletion)	cm^{-3}	0.0	$10^{19}\text{-}10^{20}$
NBL	Low body doping density	cm^{-3}	$5.0x10^{16}$	$10^{17}\text{-}10^{18}$
NBH	High body doping density	cm^{-3}	$5.0x10^{17}$	$1x10^{18}$
NDS	Source/drain doping density	cm^{-3}	$5.0x10^{19}$	$10^{19}\text{-}10^{20}$
TF	Silicon (SOI) film thickness	m	$200.x10^{-9}$	$(100\text{-}200)x10^{-9}$
TB	Effective (depleted) film thickness	m	$100.x10^{-9}$	$(25\text{-}50)x10^{-9}$
QM	Energy Quantization Parameter (0 for no quantization)	-	0.0	0-0.5
THALO	Halo thickness (0 for no halo)	m	0.0	$(50\text{-}100)x10^{-9}$
NHALO	Halo doping density	cm^{-3}	0.0	$1x10^{18}$
LRSCE	Characteristic length for reverse short-channel effect (0 for no RSCE)	m	0.0	$0.1x10^{-6}$
UO	Low-field mobility	$cm^2 \bullet V^{-1} \bullet s^{-1}$	700.	200-700 (nMOS) 70-400 (pMOS)

Table 1: UFSOI-4.5 NFD MOSFET Model Parameters

THETA	Mobility degradation coefficient	cm•V^{--1}	1.0x10^{-6}	(0.1-3)x10^{-6}
VSAT	Carrier saturated drift velocity	cm•s^{-1}	1.0x10^{7}	(0.5-1)x10^{7}
ALPHA	Impact-ionization coefficient (0 for no impact ionization)	cm^{-1}	0.0	2.45x10^{6}
BETA	Impact-ionization exponential factor	V•cm^{-1}	0.0	1.92x10^{6}
LLDD	LDD region length (0 for no LDD)	m	0.0	(0.05-0.2)x10^{-6}
NLDS	LDD/LDS doping density (>1x10^{19}: D/S extensions)	cm^{-3}	5.0x10^{19}	1x10^{19}
BGIDL	GIDL exponential factor (0 for no GIDL)	V•m^{-1}	0.0	(4-8)x10^{9}
NTR	Effective trap density for trap-assisted junction tunneling (0 for no tunneling)	cm^{-3}	0.0	10^{14}-10^{15}
JRO	Body-source/drain junction recombination current coefficient	A•m^{-1}	1.0x10^{-10}	10^{-11}-10^{-9}
M	Junction non-ideality factor	-	2.0	1-2
CGFDO	Gate-drain overlap capacitance	F•m^{-1}	0.0	1x10^{-10}
CGFSO	Gate-source overlap capacitance	F•m^{-1}	0.0	1x10^{-10}
CGFBO	Gate-body overlap capacitance	F•m^{-1}	0.0	0.0
RD	Specific drain parasitic resistance	Ω•m	0.0	(100-1000)x10^{-6}
RS	Specific source parasitic resistance	Ω•m	0.0	(100-1000)x10^{-6}
RHOB	Body sheet resistance	Ω/sq.	0.0	30x10^{3}
DL	Channel-length reduction	m	0.0	(0.05-0.15)x10^{-6}
DW	Channel-width reduction	m	0.0	(0.1-0.5)x10^{-6}
LDIFF	Effective diffusion length in source/drain	m	0.1x10^{-6}	(0.1-0.5)x10^{-6}
SEFF	Effective recombination velocity in source/drain	cm•s^{-1}	1.0x10^{5}	(0.5-5)x10^{5}
FNK	Flicker noise coefficient (0 for no flicker noise)	F•A	0.0	0-10^{-25}

Table 1: UFSOI-4.5 NFD MOSFET Model Parameters

FNA	Flicker noise exponent	-	1.0	0.5-2.0
Flag Parameters				
Name	**Description**	**Units**	**Default**	**Typical Value**
BJT	Parasitic bipolar flag (0: off; 1: on)	-	1	1
TPG	Type of gate material (+1: opposite to body; -1: same as body)	-	+1	+1
TPS	Type of substrate material (+1: opposite to body; -1: same as body)	-	-1	-1
SELFT	Self-heating flag (0: no self heating; 1: approximate model; 2: full model)	-	0	0
Optional Parameters				
Name	**Description**	**Units**	**Default**	**Typical Values**
TAUO	Carrier lifetime in lightly doped region	s	Calculated	10^{-7}-10^{-5}
VFBF	Front-gate flatband voltage	V	Calculated	-1 (nMOS) +1 (pMOS)
VFBB	Back-gate flatband voltage	V	Calculated	-
WKF	Front-gate work function difference	V	Calculated	~ **VFBF**
WKB	Back-gate work function difference	V	Calculated	-
BFACT	V_{DS}-averaging factor for mobility degradation	-	0.3	0.1-0.5
FVBJT	BJT current directional partioning factor (0 for lateral 1D flow)	-	0.0	0-1
RHOSD	Source/drain sheet resistance	Ω/sq.	0.0	50

2.1. Preliminary Model Card

We begin the calibration by defining a preliminary set of model parameters estimated directly from each device structure (**TOXF**, **TOXB**, **NSUB**, **NGATE**, **TPG**, **TPS**, **NDS**, **TF**, **TB**, **THALO** and **NHALO** (if applicable), **NBL**, **NBH**, **LLDD** and **NLDS** (if applicable), **CGFDO**,

CGFSO, **CGFBO**, **RD**, **RS**, **RB**, **RHOB, DL**, **DW**) and the pertinent device physics (**UO**, **THETA**, **VSAT**, **ALPHA**, **BETA**, **TAUO**, **JRO**, **M**, **LDIFF**, **SEFF**, **BGIDL**, **QM**, **NTR**, **LRSCE**). This estimation can be done quickly, and our experience has shown that the preliminary model card typically is a good representation of the technology, even when the device structure is not precisely known. For the AMD technology [7], with dual-polysilicon gates (n^+ poly for nMOS and p^+ poly for pMOS), the parameters given in Table 2 are defined unequivocally for both nMOS and pMOS devices. **TOXF** is the physical thickness of the gate-oxide; polysilcon-gate depletion and energy quantization are options in UFSOI-4.5. If these options are used, then we initially estimate **NGATE** to be 5.0×10^{19} and **QM** to be 0.4, where the latter is based on a general calibration of the UFSOI model to numerically simulated devices with channel doping in the range 10^{16} - 10^{18} cm^{-3} [9]. **TOXF** should be set to the measured electrical value of the oxide thickness, which is typically 10-20% thicker than the physical value, if the polysilicon-depletion and energy-quantization options are not used.

Several of the parameters listed in Table 1 are either unimportant or inapplicable for this

Table 2: Model Parameters Evaluated Directly from Technology Information

Parameter	Value
TOXF	7.0 nm
TOXB	0.36 μm
TF	0.12 μm
TPG	+1
TPS	-1, +1
W (drawn)	20 μm
L (drawn)	1.0 and 0.35 μm

technology. For example, **NQFF** is typically low enough that it is not significant in a scaled technology, and **NQFB** is generally not critical in NFD devices. **NQFSW** can be set to 0 generally, unless narrow-width effects on threshold voltage are important, in which case measured data from a narrow-W device is needed for evaluation. We can also assume for the nMOS device that the impact-ionization parameters, **ALPHA** and **BETA**, retain their physical values of 2.45×10^6 and 1.92×10^6, respectively, as confirmed experimentally for electrons [10], [11]. For the pMOS device, **ALPHA** and **BETA** are less important since the impact-ionization rate for holes is much smaller than that for electrons; they can be adequately estimated in the tuning process as we describe. Thus, there are only 17 key parameters that have to be tuned beyond their initial estimated values: **NBL**, **TF**, **TB**, **UO**, **THETA**, **VSAT**, **BGIDL**, **TAUO**, **JRO**, **M**, **RD**, **RS**, **DL**, **LRSCE**, **NGATE**, **QM** and **NTR**. The overlap capacitances, **CGFDO** and **CGFSO**, can be estimated by calculation (ε_{ox}**DL**/2**TOXF**), but should be tuned based on a measured gate C-V characteristic because of possible nonlinearities and fringing effects. The parameter tuning is done systematically as detailed in the following sections.

2.2. Long-L Calibration

First, we calibrate to long-L devices to tune **TB**, **NBL**, **NGATE**, **QM**, **NGATE**, **UO**, **THETA**, **JRO** and **M**. These evaluations are simplified since **DL**, **LRSCE**, **VSAT**, **RD** and **RS** are not significant for long L. In addition, self-heating is less significant for long L and hence can be easily avoided. Since UFSOI-4.5 accounts for carrier thermal generation throughout the channel region, the parameter evaluation for a long-L device, for which such generation can be significant, can be done easily and reliably. We choose 1.0 μm devices for the long-L calibration.

<u>Stage 1</u>

With the preliminary model parameter set, we can tune **TB** for subthreshold slope using the measured I_{DS}-V_{GfS} characteristic at low V_{DS} (no kink) as illustrated in Fig. 1. The subthreshold

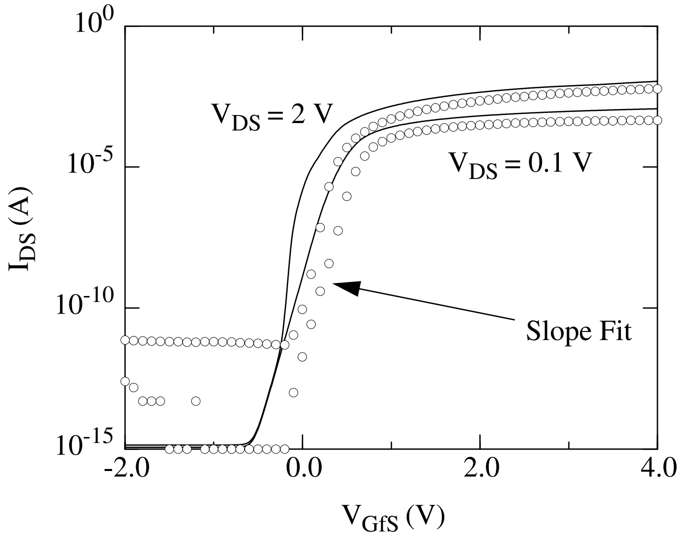


Fig. 1(a). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI nMOS device (Stage 1).

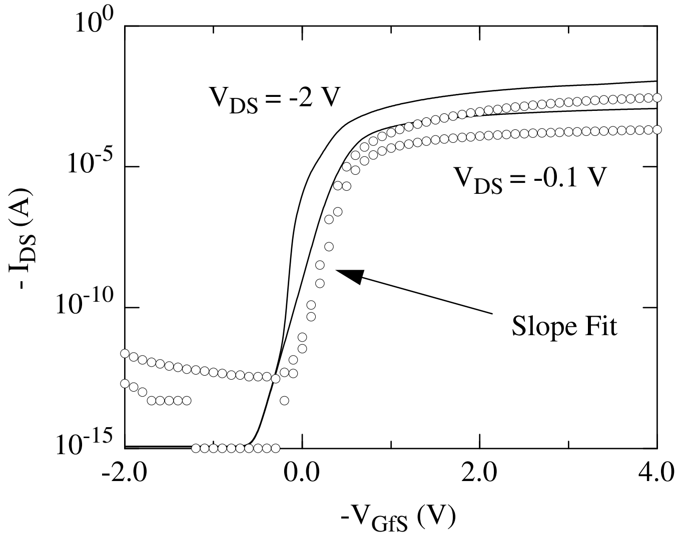


Fig. 1(b). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI pMOS device (Stage 1).

Evaluated Parameter	Measurement Data	Device
TB	I_{DS} vs. V_{GfS} @ low V_{DS} (100 mV)	Long-L

slope is given approximately as [2]

$$S \cong 60\left(1 + \frac{C_d}{C_{ox}}\right) \tag{1}$$

where $C_d \cong \varepsilon_s/\mathbf{TB}$ is the depletion capacitance and $C_{ox} = \varepsilon_{ox}/\mathbf{TOXF}$ is the gate capacitance. We thereby obtain **TB** = 58 nm for both nMOS and pMOS, which is consistent with the technology.

Stage 2

Evaluated Parameters	Measurement Data	Device
NBL (**NBH**)	I_{DS} vs. V_{GfS} @ low V_{DS} (100 mV)	Long-L

As illustrated in Fig. 2, **NBL** can be tuned to fit the subthreshold current from the I_{DS}-V_{GfS} characteristic at low V_{DS} (no kink). The subthreshold current varies inversely with **NBL**. We obtain **NBL** = 3.1 x 10^{17} cm^{-3} for nMOS and 2.5 x 10^{17} cm^{-3} for pMOS, which are also consistent with the technology. The technology does not have steep retrograded channels; we therefore assume, based on typical channel doping profiles, that **NBH** is about a factor of two higher than **NBL**. As we discuss later, the value of **NBH** can be updated based on the gate C-V characteristic.

Stage 3 (optional with **TOXF** set to electrical gate-oxide thickness)

Evaluated Parameters	Measurement Data	Device
QM, **NGATE** **(CGFSO, CGFDO)**	C_{GfS} vs. V_{GfS} @ low V_{DS} (~0 V)	Long-L (Short-L MOSC)

Calibration as well as verification via C-V characteristics are essential for reliable transient

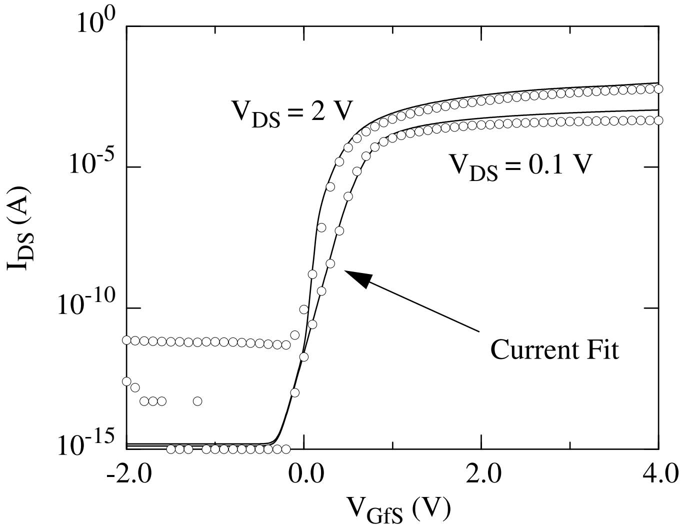


Fig. 2(a). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI nMOS device (Stage 2).

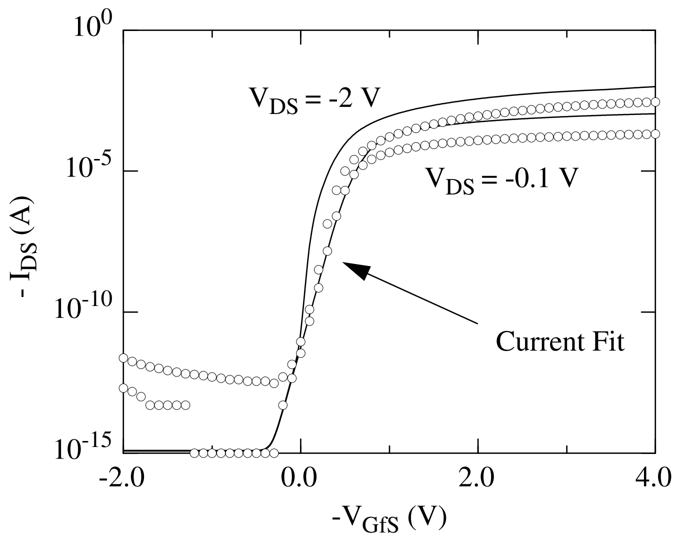
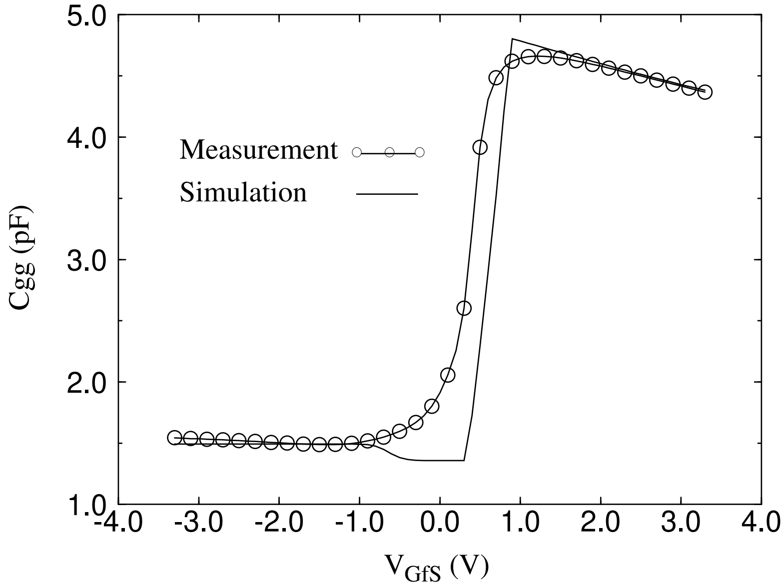


Fig. 2(b). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI pMOS device (Stage 2).

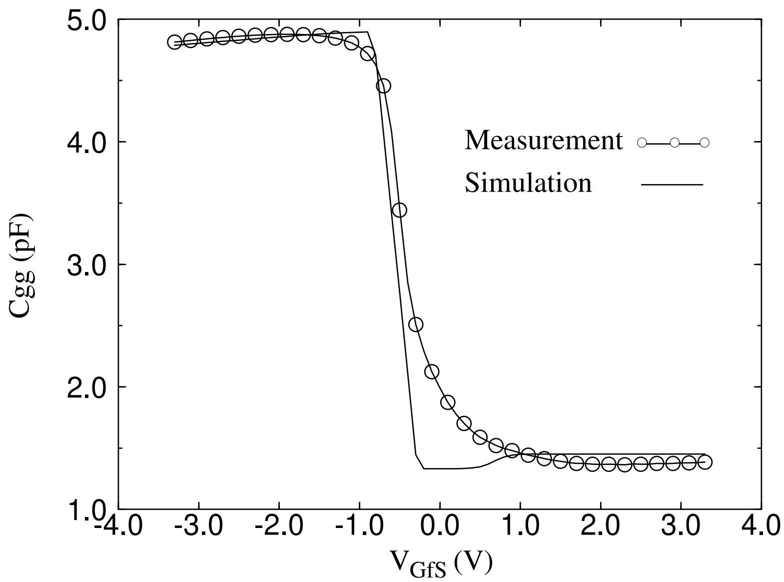
as well as AC simulations. We exemplify the C-V calibration here to lay the foundation for tuning the poly-depletion and quantization parameters of the UFSOI model, in addition to evaluating the gate-source and gate-drain overlap capacitances, **CGFSO** and **CGFDO** (from a short-L gate MOSC).

From the front-gate (-source/drain) C-V characteristic of the floating-body device, **QM** and **NGATE** can be tuned based on the estimation of capacitance lowering in strong inversion, respectively, as depicted in Fig. 3. Physically, both poly-gate depletion and energy quantization affect current and capacitances predominantly in strong inversion. Energy quantization can be important even near threshold, and hence tends to lower the subthreshold current and increase the threshold voltage. Consequently, the calibration of subthreshold current demonstrated in Stage 2 might need refinement, depending on the significance of the quantization. In this example, the gate C-V characteristics are derived from AC simulations, and the measured data [7] are taken at 1 MHz from floating-body nMOSFETs and pMOSFETs with V_{DS} = 0. The gate width and length of the devices are 2000 μm and 0.5 μm, respectively. Note that the latter is not long, and hence **CGFSO** and **CGFDO** can be tuned as well. However, to avoid the effects of overlap capacitances and **DL**, long-L devices are preferable. In this example, **NGATE** and **QM** are tuned as 2.0 x 10^{19} cm^{-3} and 0.45, respectively, for nMOS, and 7.5 x 10^{19} cm^{-3} and 0.4, respectively, for pMOS. Note that the nMOS characteristic implies a flatband voltage that is slightly different from that of the devices used to calibrate the model.

In addition, other parameters can be either evaluated or verified via the C-V characteristic in the accumulation region. As indicated in Fig. 3, floating-body effects are apparent and must be accounted for. The floating body is capacitively coupled to the gate, but the hole charge in the body cannot respond at the high frequency; hence the source/drain junction capacitance becomes important in the accumulation region. Examination of the measured and simulated C-V



(a)



(b)

Fig. 3. C-V characteristics of L/W = 0.5μm/2000μm floating-body NFD/SOI MOSFETs; f = 1 MHz, V_{DS} = 0 V: (a) nMOS, (b) pMOS.

characteristics in different gate-bias regions gives good insight on the floating-body effects and lends support to the UFSOI basic charge/capacitance modeling and calibration. In the accumulation region, the relatively low capacitance, in contrast to that of a tied-body device, reflects the predominant source and drain junction capacitances, as well as overlap capacitances. In this region then, **NBH** and **TF** can be refined, and the overlap capacitances can be tuned. We find that **CGFDO** and **CGFSO** are effective values, larger than ε_{ox}**DL/2TOXF**, because of the fringing components not accounted for explicitly in the UFSOI model. **NBH** and **TF** influence the low capacitance in the accumulation region, but not as much as **CGFDO** and **CGFSO**.

<u>Stage 4</u>

Evaluated Parameters	Measurement Data	Device
JRO, **TAUO**, **M**, **BGIDL**, **NTR** **ALPHA**, **BETA** (pMOS)	I_{DS} vs. V_{GfS} @ high V_{DS} (2.0 V)	Long-L

If GIDL is not prevalent, **JRO** and **M** can be evaluated from the drain-induced shift in current (without kink) and the slope (with kink), respectively, of the I_{DS}-V_{GfS} characteristic at high V_{DS}, as demonstrated in Fig. 4. The shift in current is due in part to DIBL, modeled internally, but mainly it is due to the floating-body effect, i.e., the induced $V_{BS} > 0$ caused by injection (e.g., generation) of majority carriers into the body. The DC V_{BS} is defined by the balance of the carrier generation from the body-drain junction and recombination from the body-source junction as well as the quasi-neutral source. The recombination current is modeled as [3]

$$I_R(V_{BS}) = W\mathbf{JRO}\exp\left(\frac{V_{BS}}{\mathbf{M}V_T}\right) + W\mathbf{TF}\frac{qn_i^2}{N_{DS(eff)}}\mathbf{SEFF}\exp\left(\frac{V_{BS}}{V_T}\right) \qquad (2)$$

where the first term tends to be predominant in this context. Thus, if the generation current (due to impact ionization here) is characterized well, **M** and **JRO** can be evaluated from the high-V_{DS} subthreshold I_{DS}-V_{GfS} characteristic. However, the generation current can have more than one

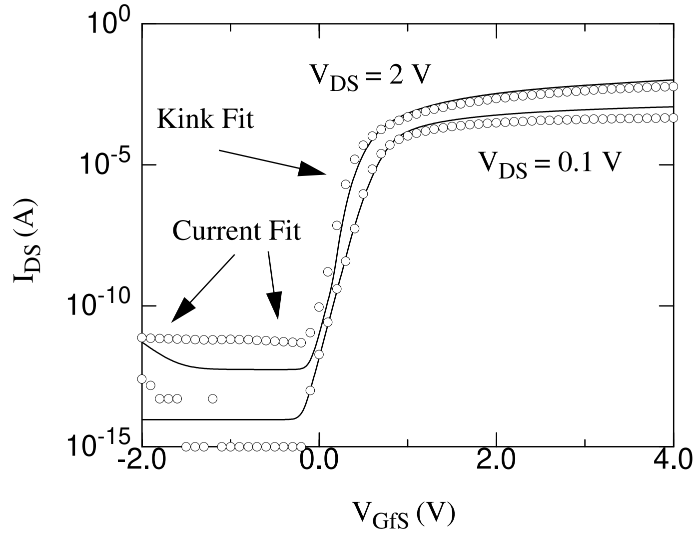


Fig. 4(a). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI nMOS device (Stage 4).

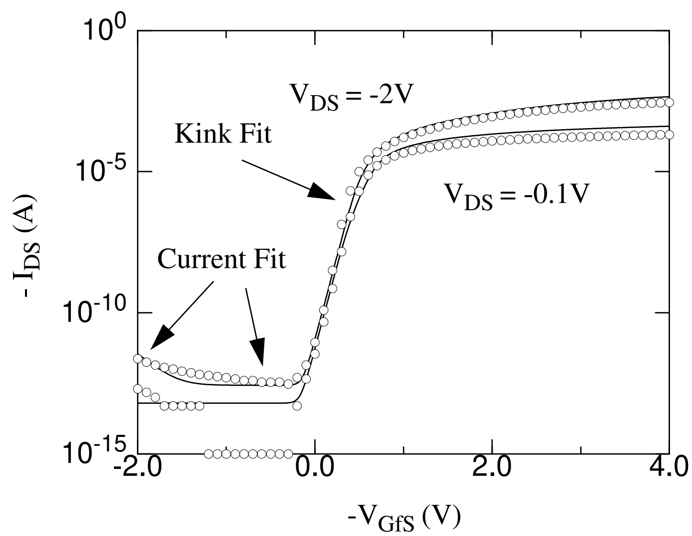


Fig. 4(b). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI pMOS device (Stage 4).

component, and hence the general evaluation will usually involve other parameters associated with it as well. In fact, GIDL can influence the off-state leakage current near the kink. We hence include **BGIDL** evaluation in this stage, knowing that it is independent of L.

For scaled devices, the thermal generation should correlate with the thermal recombination. Hence, the value of **TAUO** should be loosely correlated with **JRO** in accord with basic pn-junction recombination/generation properties as follows:

$$\mathbf{JRO} \cong \frac{qn_i\mathbf{TF}y_d}{\tau_r} \tag{3}$$

and

$$\tau_r \cong \tau_g \cong \frac{2\mathbf{TAUO}}{1 + \mathbf{NBH}/\mathbf{N_O}} \tag{4}$$

where y_d, typically ~50 nm, is a junction space charge-region width, and N_O is $5\text{x}10^{16}$ cm^{-3}. With (3) and (4), **TAUO** calculated from the default **JRO** ($1.0\text{x}10^{-10}$ A•m^{-1}) is on the order of 1 μs, which is physically consistent with recent technologies. In UFSOI-4.5, **TAUO** is defaulted to 0 and used as a flag for internal calculation of the generation current, based only on **JRO** as indicated by (3) and (4). However, for long-L devices, the generation current from the channel/ body region will require tuning of **TAUO**, which is done as described herein.

We suggest that **BGIDL** first be tuned to fit GIDL current of the I_{DS}-V_{GfS} characteristic at high V_{DS} and $V_{GfS} < 0$ (where GIDL is most significant) for nMOS, as demonstrated in Fig. 4(a), using an estimated **DL** from the technology. Then we tune **JRO** to calibrate the pre-kink region of the high-V_{DS} curve, and tune **M** to set the kink effect, as well as fine-tune the pre-kink region in conjunction with **JRO**. This calibration is illustrated in Fig 4(a). Once **JRO** is obtained, **TAUO** (for the long-L device) can be first estimated using (3) and (4), and then tuned as described in Stage 6. In the $V_{GfS} < 0$ region of the high-V_{DS} I_{DS}-V_{GfS} characteristic, we can tune the junction-tunneling parameter, **NTR**, in conjunction with **BGIDL** to match the leakage current if it is under-predicted by accounting for the thermal generation. A few iterations on the values of these parameters may be necessary; **BGIDL** should be iterated too if GIDL seems important near the subthreshold kink. (Because a weighting factor is used in the characterization of the source/drain junction recombination/generation currents to ensure symmetry, varying **TAUO** can cause a slight variation in the long-L model characteristic in the pre-kink region.)

As was mentioned previously, the impact-ionization rate for holes is much smaller than that for electrons. Since there is no clear indication of the values of **ALPHA** and **BETA** for holes in the literature, they should also be tuned for pMOS, along with **JRO**, from the kink shown by the data in Fig. 4(b). If we increase **BETA**, the onset voltage of the kink will be pushed out. (**ALPHA** and **BETA** can also be checked later to match the kinks of I_{DS} -V_{DS} characteristics, as plotted in Fig. 6.) We obtain **JRO** = 1.0 x 10^{-10} A/m, **TAUO** = 1.0 x 10^{-6} s, **M** = 1.5, **BGIDL** = 4.5 x 10^{9} V•m^{-1}, and **NTR** = 4.5 x 10^{14} cm^{-3} for nMOS (with **ALPHA** and **BETA** given previously), and **JRO** = 1.0 x 10^{-10} A/m, **TAUO** = 1.0 x 10^{-6} s, **M** = 1.5, **BGIDL** = 4.6 x 10^{9} V•m^{-1}, **ALPHA** = 2.45 x 10^{6} cm^{-1}, **BETA** = 3.0 x 10^{6} V/cm, and **NTR** = 9.0 x 10^{14} cm^{-3} for pMOS.

Note in Fig. 4 that the long-L devices, especially nMOS, show anomalous leakage current at high V_{DS} near V_{GfS} = 0. This current, which in fact varies substantially in different devices from the technology, can influence the drain-induced floating-body effect on off-state current as well as subthreshold kink as indicated in Fig. 4(a). Furthermore, it can undermine the accuracy of calibrated parameters. Therefore, **BGIDL** and **NTR** for nMOS were evaluated using the short-L device I_{DS}-V_{GfS} characteristic, as shown in Fig. 7(a).

Stage 5

Evaluated Parameters	Measurement Data	Device
UO, **THETA**	I_{DS} vs. V_{GfS} @ low V_{DS} (100 mV)	Long-L

From the I_{DS}-V_{GfS} characteristic at low V_{DS}, **UO** and **THETA** can be tuned directly, as indicated in Fig. 5, since **RD** and **RS** are not significant here for long L. The low (longitudinal)-field mobility is dependent on the transverse field (E_x) in the channel, which is modeled by the average field as

$$\mu_{eff} = \frac{\mathbf{UO}}{1 + \mathbf{THETA}\bar{E}_x(y)} . \tag{5}$$

In this calibration, some iterations are required, but the optimization is not complex. (An alternative methodology that can be used is based on g_m-V_{GfS} at low V_{DS}, as shown in Figs. 12(a) and 13(a).) The calibration should be precise here, even though the short-L tuning will alter the parameter values somewhat. We obtain **UO** = 800 cm^2/V/s and **THETA** = 2.3 x 10^{-6} cm/V for nMOS, and **UO** = 250 cm^2/V/s and **THETA** = 1.9 x 10^{-6} cm/V for pMOS.

Stage 6

Evaluated Parameter	Measurement Data	Device
TAUO, **NTR**	I_{DS} vs. V_{DS} @ low V_{GfS} (~1 V)	Long-L

Since **TAUO** has been initially estimated in Stage 4, we only need to fine-tune the value to negate possible inaccuracies of approximations, e.g., $\tau_r \cong \tau_g$. The fine-tuning serves as a verification of the **JRO**-defined **TAUO** as well.

Large changes in **TAUO** should not be allowed here; such changes would reflect another current component, e.g., due to junction trap-assisted tunneling, which can be used to tune the

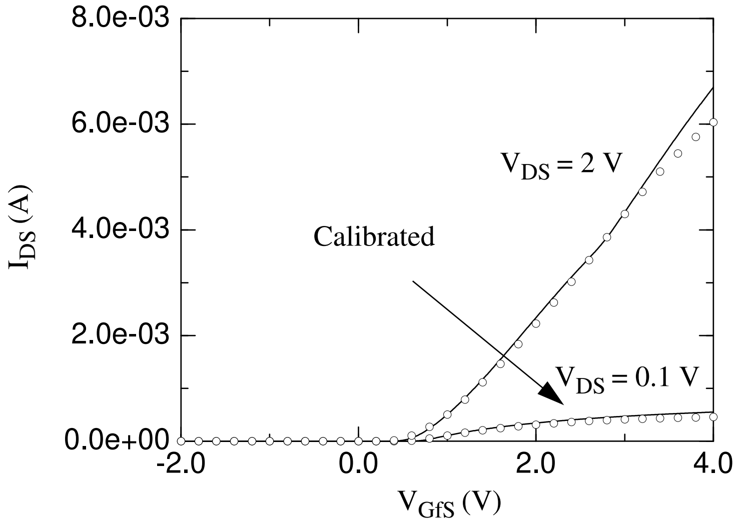


Fig. 5(a). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SOI nMOS device (Stage 5).

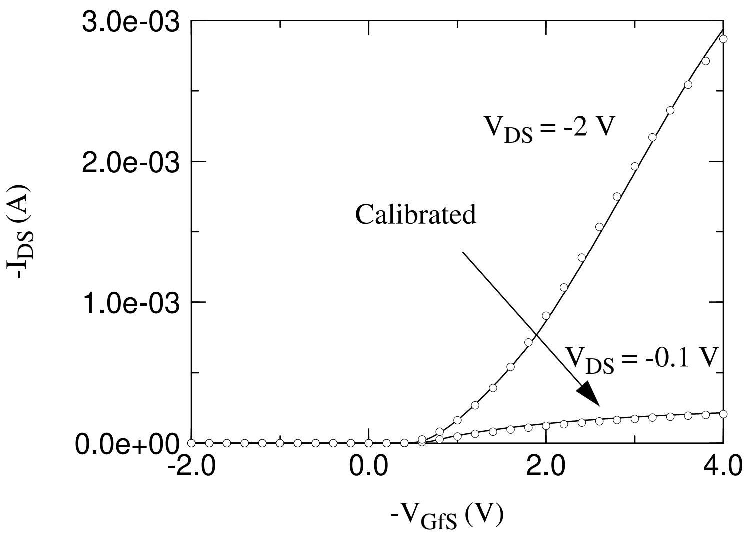


Fig. 5(b). I_{DS} -V_{GfS} characteristics of 1.0 μm NFD/SO pMOS device (Stage 5).

effective trap density, **NTR**. Fig. 6 shows the refining of **TAUO** from I_{DS} -V_{DS} characteristics at V_{DS} ~ $V_{DS(sat)}$ (no kink) and low V_{GfS} where I_{DS}(sat) is controlled by pinch-off and where it reflects clearly the threshold lowering due to the thermal generation current-driven floating-body effect. If we see the current increasing with V_{DS} in this same region, then we will have to tune **NTR**. The effects of carrier velocity saturation (**VSAT**) at higher V_{GfS}, which will be discussed later, should be avoided here. The values of **TAUO** and **NTR** evaluated in Stage 4 are still valid here.

2.3. Short-L Calibration

The parameter set obtained from the long-L device tuning is now used to initiate the tuning from the short-L (target) device. The short-L calibration is similar to that described for long L, but with some additional parameters. In fact, if long-L data is not available, the calibration could be done with the short-L data only, albeit with a bit more complexity. Self-heating is usually more prevalent in short-L device data, so it must be cautiously avoided for reliable parameter evaluation. (The UFSOI models do have a self-heating option [5], [12], which uses two additional parameters (**RTH** and **CTH**) that could be tuned. However, a reliable calibration can be done without considering self-heating.) The remaining parameters to be evaluated from the short-L device data are **DL**, **RD**, **RS**, **VSAT**, and **LRSCE**.

<u>Stage 7</u>

Evaluated Parameters	Measurement Data	Device
DL, **LRSCE**	I_{DS} vs. V_{GfS} @ low V_{DS} (100 mV) and high V_{DS} (2.0 V)	Short-L

If the technology shows significant reverse short-channel effect (RSCE), then the effective channel doping in the short-L device will be higher than NBL obtained from the long-L device,

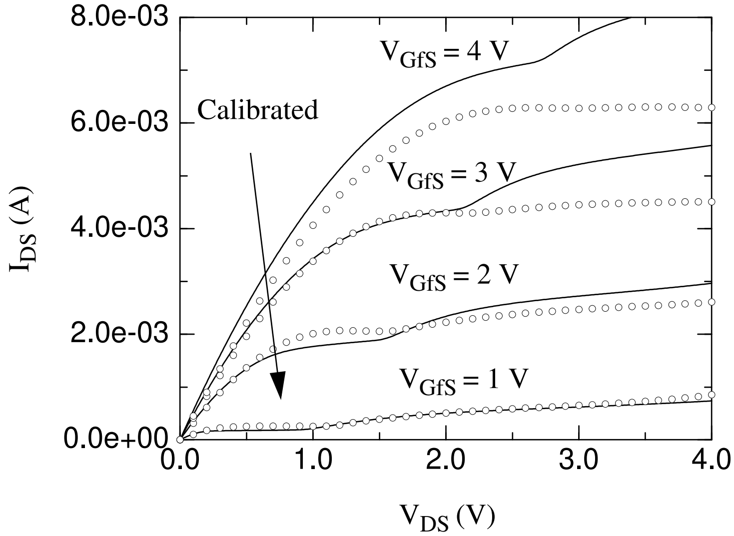


Fig. 6(a). I_{DS} -V_{DS} characteristics of 1.0 μm NFD/SOI nMOS device (Stage 6).

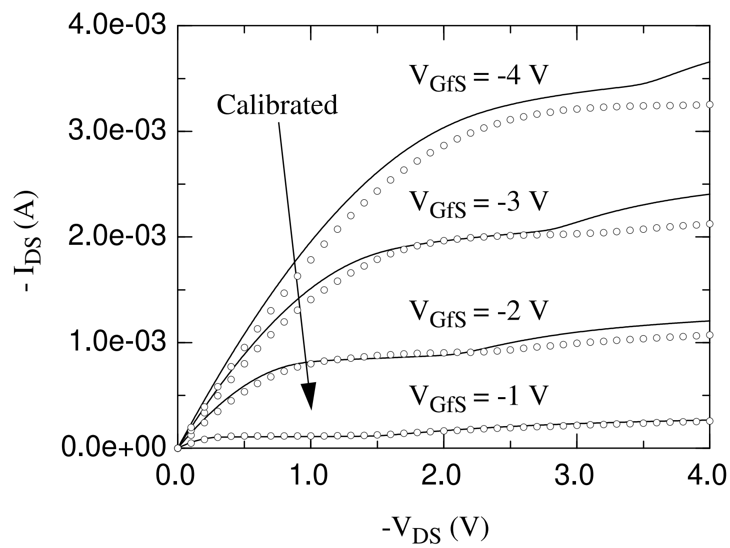


Fig. 6(b). I_{DS} -V_{DS} characteristics of 1.0 μm NFD/SOI pMOS device (Stage 6).

and the general validity of the calibration would be invalidated. Therefore, LRSCE needs to be tuned here to retain the model scalability.

Using the model parameter set we have at this point, we find that the short-L model gives the same subthreshold slope as seen in the low-V_{DS} I_{DS} -V_{GfS} data, which implies good **TB**. Since, we do not see any RSCE in this example, we hence can easily obtain **DL** by fitting the short-channel effect (DIBL) from the I_{DS} -V_{GfS} characteristics as shown in Fig. 7. In other cases, however, the short-L data may show a higher threshold voltage, implying that RSCE must be accounted for. In order to evaluate **DL** and **LRSCE** independently, we tune (refine) **LRSCE** to fit the subthreshold current, which strongly depends upon doping, and we tune (refine) **DL** to match DIBL from the I_{DS} -V_{GfS} characteristics as shown in Fig. 7. (Note that when **LRSCE** > 0, **NHALO** or **NBH** can affect the effective channel doping through a physical link modeled in UFSOI-4.5.) We obtain **DL** = 0.07 μm for nMOS and 0.08 μm for pMOS, which are consistent with the technology, and **LRSCE** = 0.0 μm for both nMOS and pMOS. Once **DL** is tuned, we may skip further **NBL**, **JRO**, **M**, **ALPHA**, and **BETA** tuning if no discrepancies are seen in the characteristics; otherwise some fine-tuning is needed.

Stage 8

Evaluated Parameters	Measurement Data	Device
RD, **RS**	I_{DS} vs. V_{GfS} @ low V_{DS} (100 mV)	Short-L

As can be seen in Fig. 8, RD and RS are evaluated from the linear region of the I_{DS} -V_{GfS} characteristics where the equivalent ON resistance is given approximately by

$$R_{ON} \equiv \frac{V_{DS}}{I_{DS}} \cong \frac{\mathbf{RS} + \mathbf{RD}}{W} + \frac{L - \mathbf{DL}}{WC_{of}(V_{GfS} - V_T)\mu_{eff}(\mathbf{UO}, \mathbf{THETA})}. \tag{6}$$

Since **RS** = **RD** due to device symmetry and **UO** and **THETA** have been tuned previously, this

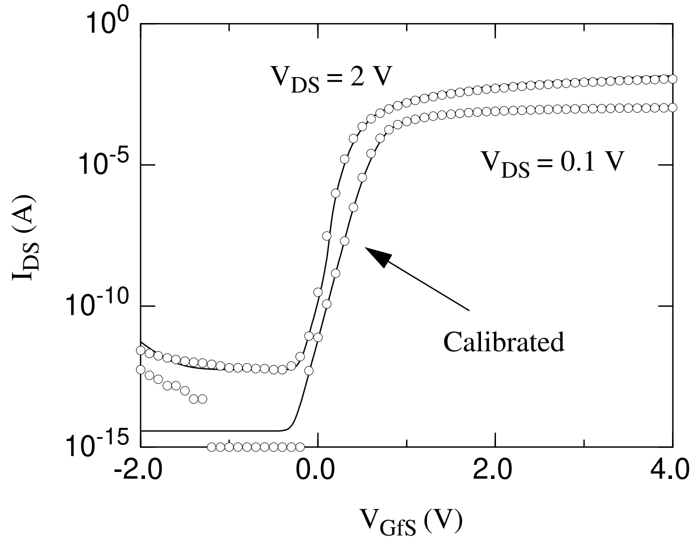


Fig. 7(a). I_{DS} -V_{GfS} characteristics of 0.35 μm NFD/SOI nMOS device (Stage 7).

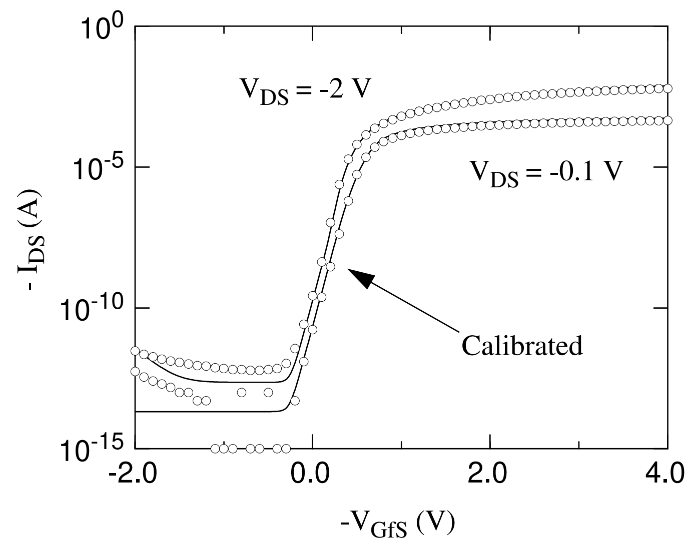


Fig. 7(b). I_{DS} -V_{GfS} characteristics of 0.35 μm NFD/SOI pMOS device (Stage 7).

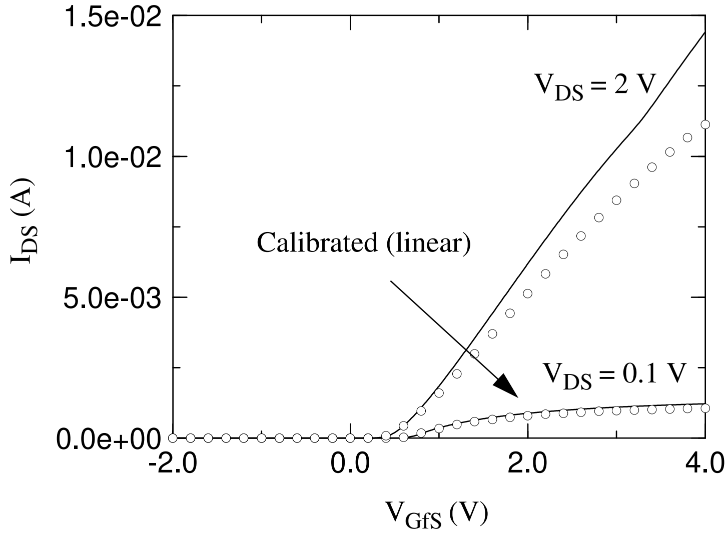


Fig. 8(a). I_{DS} -V_{GfS} characteristics of 0.35 μm NFD/SOI nMOS device (Stage 8).

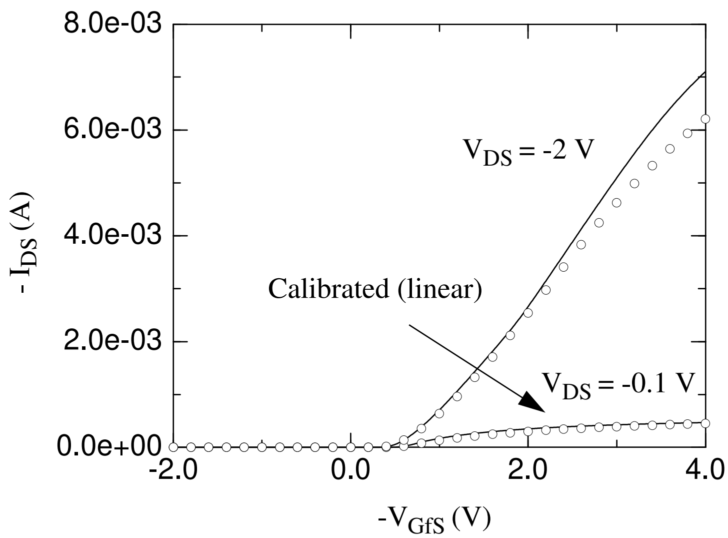


Fig. 8(b). I_{DS} -V_{GfS} characteristics of 0.35 μm NFD/SOI pMOS device (Stage 8).

evaluation is straightforward without iteration. (Note: Since **RS/RD** could have been of some importance in the long-L device, **UO** and **THETA** can be fine-tuned here to sustain the agreement with the long-L data.) Hence **RS/RD** is tuned as 400 x 10^{-6} Ω-m for nMOS and 1100 x 10^{-6} Ω-m for pMOS.

<u>Stage 9</u>

Evaluated Parameter	Measurement Data	Device
VSAT	I_{DS} vs. V_{DS} @ low power region	Short-L

Fig. 9 shows that we can tune **VSAT** from the I_{DS}-V_{DS} characteristic at high V_{GfS} with V_{DS} ~ V_{DS}(sat), where the saturation is governed by velocity saturation and not pinch-off of the channel charge (Q_c). In this case, the saturation current is expressed as [2]

$$I_{CH(sat)} = -W\mathbf{VSAT}Q_c(L)\,. \tag{7}$$

As indicated in the figure, device self-heating can and must be avoided while tuning **VSAT**. If V_{GfS} is set too high, then the power dissipation will be too high, and the self-heating will distort the data as evident in Fig. 9; if V_{GfS} is set too low, then (7) will not apply. **VSAT** is tuned to 0.8 x 10^7 cm/s for nMOS and 0.9 x 10^7 cm/s for pMOS.

2.4. Verification (Self-Heating)

After the key parameters have been tuned, both short- and long-L devices should be simulated with the single set of model parameters for verification. Further, the self-heating option [5] can be turned on for a more comprehensive comparison, after having evaluated the thermal-resistance parameter, **RTH**, via tuning to the short-L device in the high-power regions. In general, if the self heating (ΔT) exceeds ~20 ^oC, where [12]

$$\Delta T = RTH \bullet P \tag{8}$$

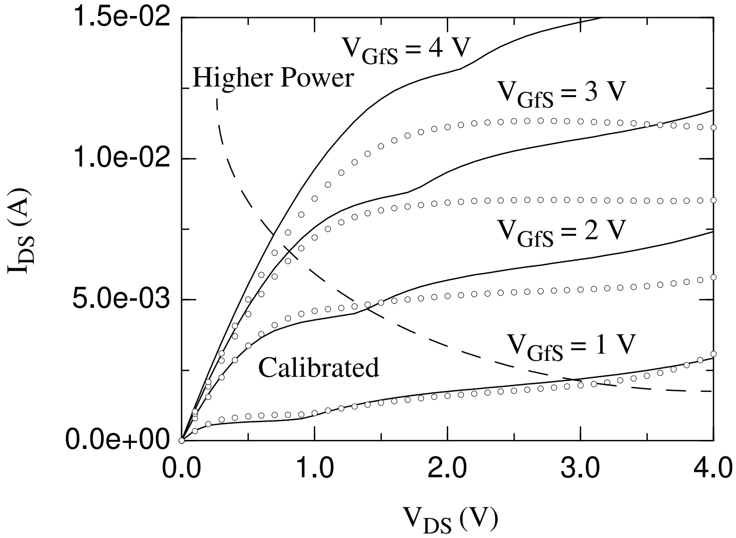


Fig. 9(a). I_{DS} -V_{DS} characteristics of 0.35 μm NFD/SOI nMOS device (Stage 9).

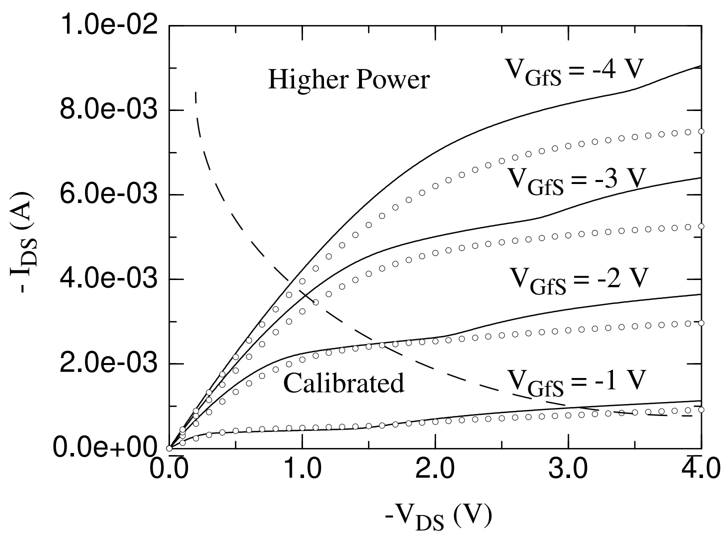


Fig. 9(b). I_{DS} -V_{DS} characteristics of 0.35 μm NFD/SOI pMOS device (Stage 9).

and

$$P = V_{DS}I_{DS} \cong V_{D'S'}(I_{CH} + I_{BJT}) + (I_{CH} + I_{BJT})^2(R_S + R_D + R_{LDS} + R_{LDD}), \tag{9}$$

then self-heating effects should be taken into account. For this technology, with L = 0.35 μm, **RTH** is derived from high-P data as 4.5 K/W for nMOS and 2.5 K/W for pMOS. With L = 1.0 μm, **RTH** is derived as 2.2 K/W for nMOS, and ignored for pMOS due to less power consumption. Although the self-heating effects can prevail in the long-L device too, they tend to be less significant since **RTH** varies inversely with device size.

For a more complete calibration, some parameters may be tuned based on additional measured data. For example, following [3] the bipolar-related source/drain parameters **SEFF** and **LDIFF** can be evaluated from transient $I_{BJT}(t)$ data. If such transient data is not available, **SEFF** can also be estimated from the kink in the I_{DS}-V_{DS} characteristics at lower V_{GfS} where it influences recombination and hence the kink current level. Finally, by matching the breakdown voltage in the I_{DS}-V_{DS} characteristics, **FVBJT** and **NBH** can be tuned.

The characteristics reflecting the final calibration of the NFD model to the AMD SOI CMOS technology are plotted in Figs. 10 and 11; the self-heating option was used in the L = 0.35 μm device simulations. Overall the model predictions match the measured data well, except for the anomalous leakage currents at $V_{GfS} < 0$ in Fig. 10(d) which, as mentioned previously, could vary substantially in different devices from the technology. In Fig. 10(f), there are discrepancies in the I_{DS}-V_{DS} characteristics in and around the kink regions; the data show less abrupt kinks. The anomalous leakage currents mentioned above, which could become predominant in charging the floating body, could also underlie these discrepancies. They might also be due to near-FD conditions induced by the bias. Such conditions are suggested by the loss of the kink with increasing V_{GfS} shown by the characteristics in Fig. 10(c) for the short-L device, in which

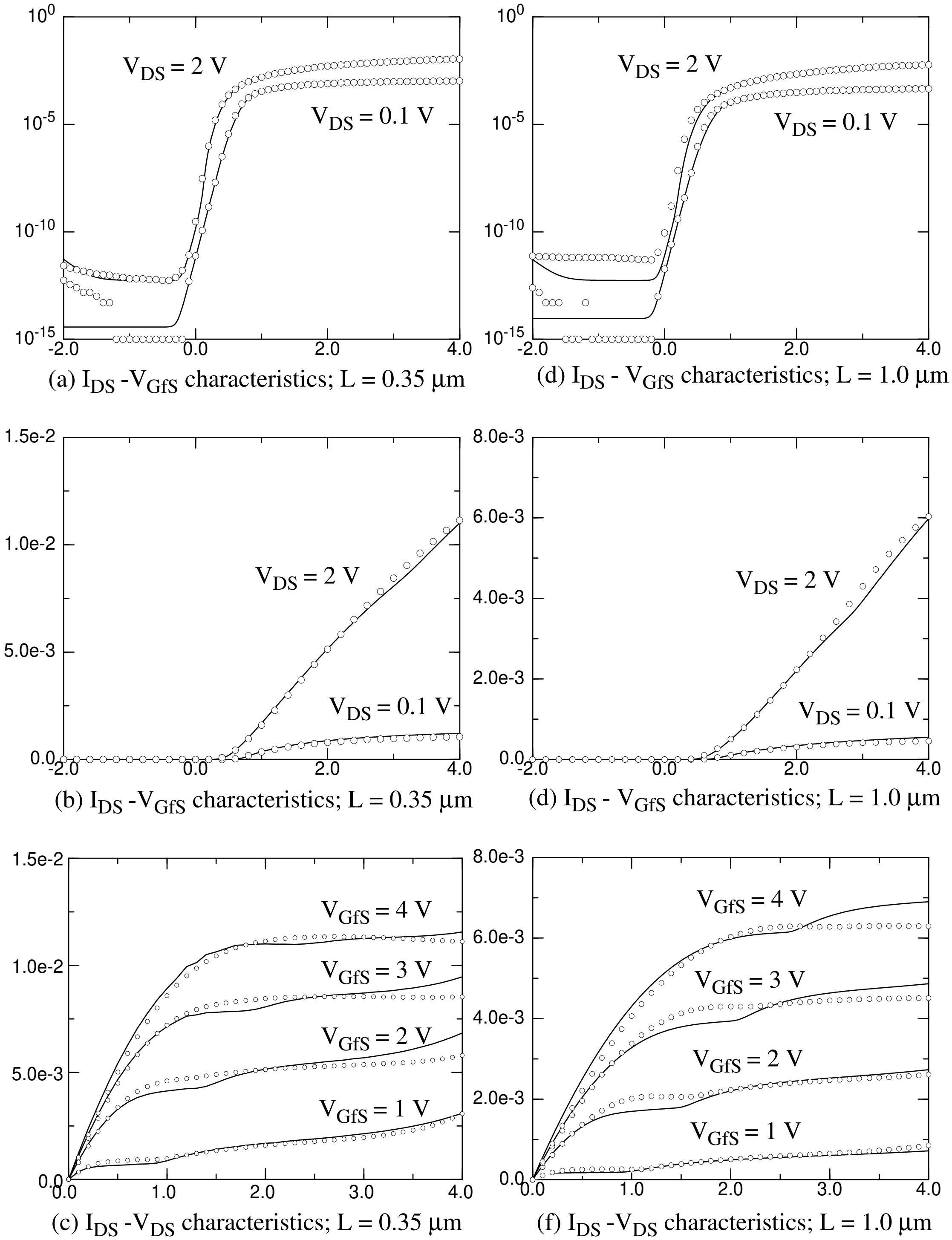
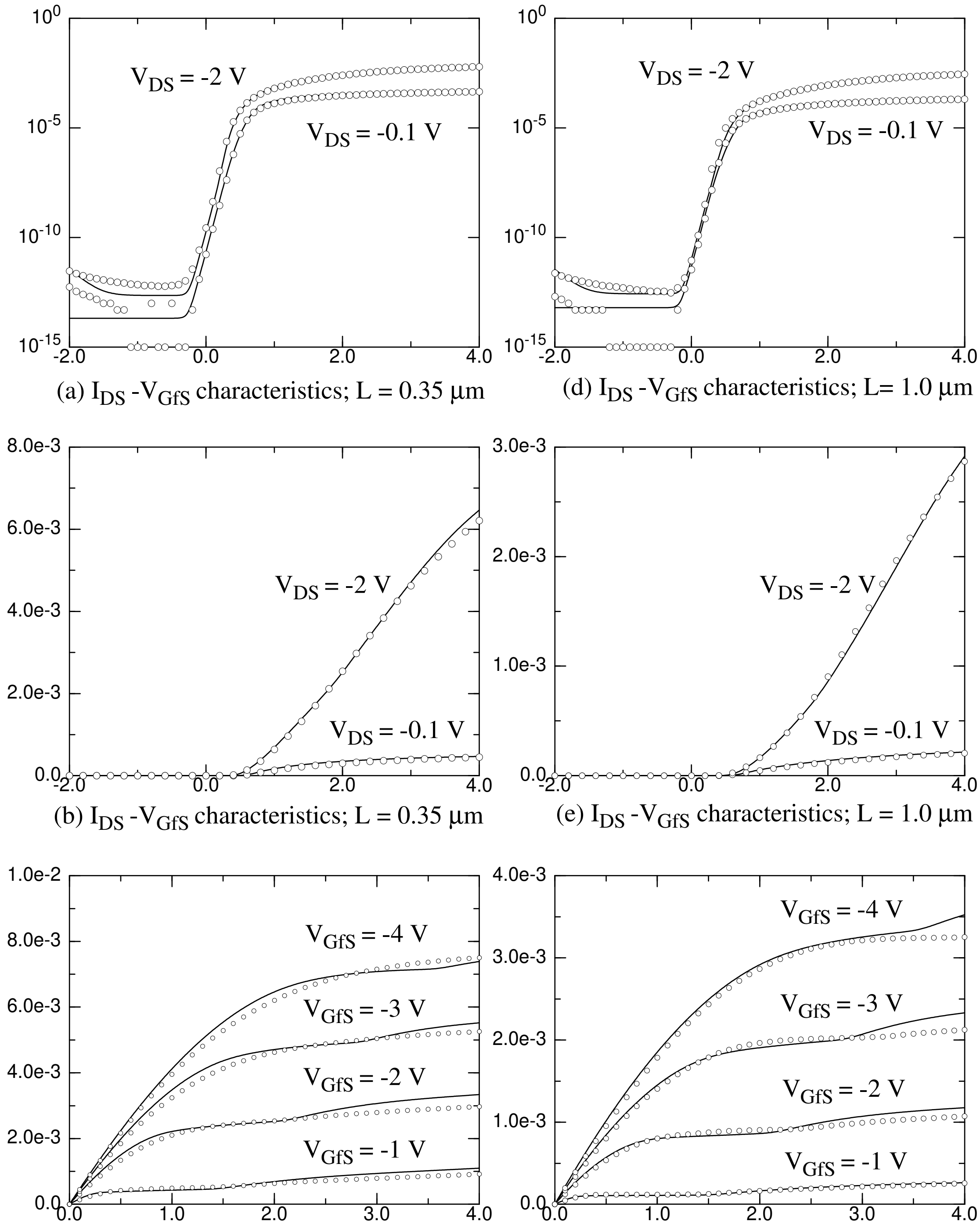


Fig. 10. Calibrated I(A) - V(V) characteristics of NFD/SOI nMOS devices.



(a) I_{DS} -V_{GfS} characteristics; L = 0.35 μm

(d) I_{DS} -V_{GfS} characteristics; L= 1.0 μm

(b) I_{DS} -V_{GfS} characteristics; L = 0.35 μm

(e) I_{DS} -V_{GfS} characteristics; L = 1.0 μm

(c) I_{DS} -V_{DS} characteristics; L = 0.35 μm

(f) I_{DS} -V_{DS} characteristics; L = 1.0 μm

Fig. 11. Calibrated I(A) - V(V) characteristics of NFD/SOI pMOS devices.

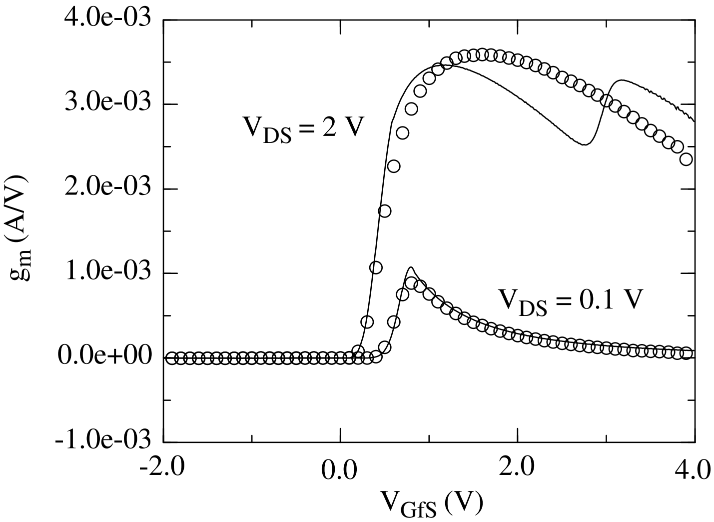
source/drain charge sharing could be supporting full depletion of the body. Figures 12 and 13 show corresponding simulated and measured conductances; the agreement is very good, although the predicted kinks in g_m are too sharp as in Figs. 10 and 11. The nMOS and pMOS model parameters derived for the target channel length are listed in Table 3. Unlisted parameters are either inapplicable or unimportant, and are set with their default values. With the parameters evaluated and tuned as described herein, the UFSOI NFD model should reliably predict not only the DC but also the transient and AC characteristics of devices and circuits from the AMD 0.35µm SOI CMOS technology.

3. Parameter Evaluation for FD/SOI MOSFETs

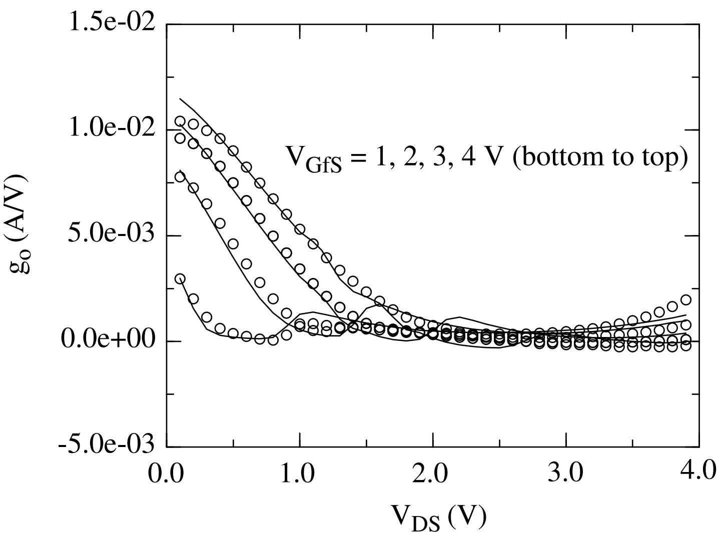
The UFSOI model parameter evaluation for FD MOSFETs also exploits the process-based nature of the model. The methodology is similar to that described for the UFSOI NFD model. The bipolar-related and impact-ionization parameters are evaluated identically. Since the FD device is somewhat immune to floating-body effects, parameters associated with them are less important. However, the FD channel-current formalism in weak inversion is more complex, accounting for 2-D fringing fields in the buried oxide (BOX) emanating from the source/drain junctions [1], [13]; two additional parameters for this effect must be tuned. The Ver. 4.5 model parameters, along with their descriptions and typical values, are listed in Table 4 [5].

3.1. Preliminary Model Card

We begin the calibration by defining a preliminary model card for each device with the parameters estimated directly from the device structure (**TOXF**, **TOXB**, **NSUB**, **NGATE**, **TPG**, **TPS**, **NDS**, **TB**, **NBODY**, **LLDD** and **NLDS** (if applicable), **CGFDO**, **CGFSO**, **CGFBO**, **RD**, **RS**, **RB**, **DL**, **DW**) and the pertinent device physics (**NSF**, **NSB**, **GAMMA**, **KAPPA**, **UO**, **THETA**, **VSAT**, **ALPHA**, **BETA**, **TAUO**, **JRO**, **M**, **LDIFF**, **SEFF**, **BGIDL**, **QM, LRSCE**). To

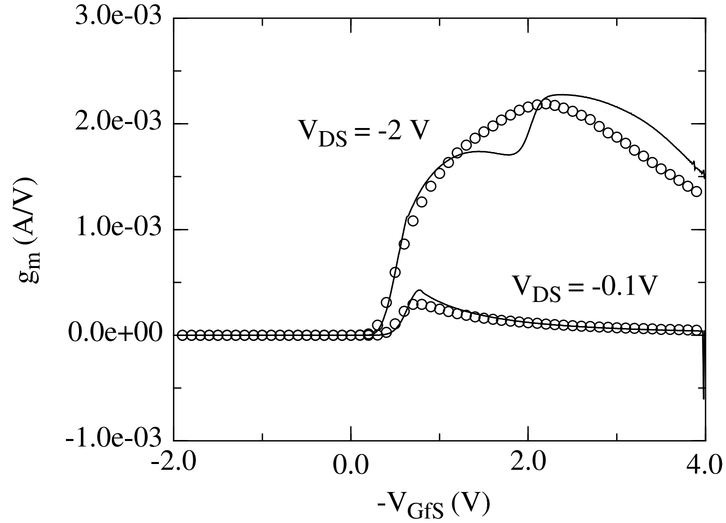


(a) Transconductance; L = 0.35 μm

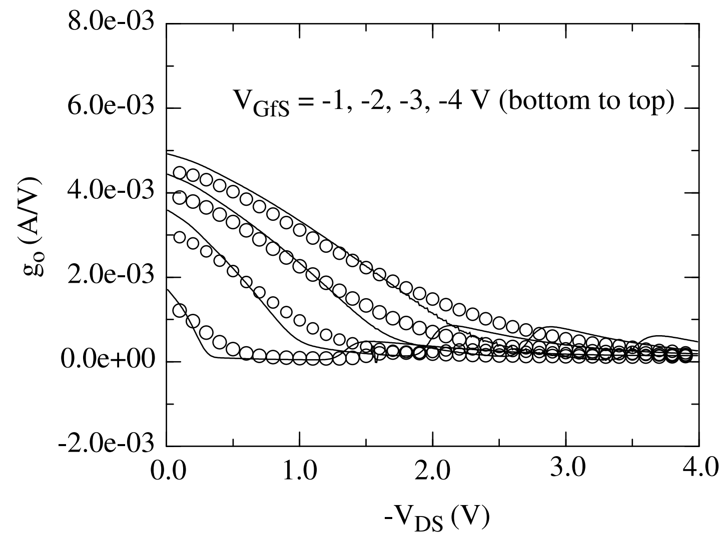


(b) Output conductance; L = 0.35 μm

Fig. 12. Calibrated conductances of NFD/SOI nMOS device.



(a) Transconductance; L = 0.35 μm



(b) Output conductance; L = 0.35 μm

Fig. 13. Calibrated conductances of NFD/SOI pMOS device.

Table 3: Evaluated Key Parameters for AMD's 0.35μm NFD/SOI CMOS Devices

Parameters	nMOS	pMOS
TOXF	7.0 nm	7.0 nm
TOXB	0.36 μm	0.36 μm
TB	0.058 μm	0.058 μm
TF	0.12 μm	0.12 μm
NBL	3.1×10^{17} cm^{-3}	2.5×10^{17} cm^{-3}
NBH	5.0×10^{17} cm^{-3}	4.0×10^{17} cm^{-3}
UO	800. cm^2/V/s	250. cm^2/V/s
THETA	2.3×10^{-6} cm/V	1.9×10^{-6} cm/V
VSAT	0.8×10^{7} cm/s	0.9×10^{7} cm/s
TPG	1	1
TPS	-1	1
ALPHA	2.45×10^{6} cm^{-1}	2.45×10^{6} cm^{-1}
BETA	1.92×10^{6} V/cm	3.0×10^{6} V/cm
RD	$400. \times 10^{-6}$ Ω-m	$1100. \times 10^{-6}$ Ω-m
RS	$400. \times 10^{-6}$ Ω-m	$1100. \times 10^{-6}$ Ω-m
TAUO	1.0×10^{-6} s	1.0×10^{-7} s
JRO	1.0×10^{-10} A/m	1.0×10^{-10} A/m
M	1.5	1.5
BGIDL	4.5×10^{9} V/m	4.6×10^{9} V/m
NTR	4.5×10^{14} cm^{-3}	9.0×10^{14} cm^{-3}
DL	0.07 μm	0.08 μm
LRSCE	0.0 μm	0.0 μm
SEFF	9.0×10^{5} cm/s	7.0×10^{5} cm/s
NGATE	2.0×10^{19} cm^{-3}	7.5×10^{19} cm^{-3}
QM	0.45	0.4
CGFSO	0.245×10^{-9} F/m	0.245×10^{-9} F/m
CGFDO	0.245×10^{-9} F/m	0.245×10^{-9} F/m

Table 4: UFSOI-4.5 FD MOSFET Model Parameters

Name	Description	Units	Default	Typical Values
NQFF	Front oxide fixed charge	cm^{-2}	0.0	~ 10^{10}
NQFB	Back oxide fixed charge	cm^{-2}	0.0	~ 10^{11}
NQFSW	Sidewall fixed charge (normalized) (0 for no narrow-width effect)	cm^{-2}	0.0	$\pm 10^{12}$
NSF	Front surface state charge density	cm^{-2}	0.0	~ 10^{10}
NSB	Back surface state charge density	cm^{-2}	0.0	~ 10^{11}
TOXF	Front-gate oxide thickness	m	$10.x10^{-9}$	$(3\text{-}8)x10^{-9}$
TOXB	Back-gate oxide thickness	m	$500.x10^{-9}$	$(80\text{-}400)x10^{-9}$
NSUB	Substrate doping density	cm^{-3}	$1.0x10^{-15}$	$10^{15}\text{-}10^{17}$
NGATE	Poly-gate doping density (0 for no poly-gate depletion)	cm^{-3}	0.0	$10^{19}\text{-}10^{20}$
NBODY	Film (body) doping density	cm^{-3}	$5.0x10^{16}$	$10^{17}\text{-}10^{18}$
NDS	Source/drain doping density	cm^{-3}	$5.0x10^{19}$	$10^{19}\text{-}10^{20}$
TB	Film (body) thickness	m	$100.x10^{-9}$	$(30\text{-}100)x10^{-9}$
QM	Energy Quantization Parameter (0 for no quantization)	-	0.0	0-0.5
UO	Low-field mobility	$cm^2 \bullet V^{-1} \bullet s^{-1}$	700.	200-700 (nMOS) 70-400(pMOS)
THETA	Mobility degradation coefficient	$cm \bullet V^{--1}$	$1.0x10^{-6}$	$(0.1\text{-}3)x10^{-6}$
VSAT	Carrier saturated drift velocity	$cm \bullet s^{-1}$	$1.0x10^{7}$	$(0.5\text{-}1)x10^{7}$
ALPHA	Impact-ionization parameter a_0	cm^{-1}	0.0	$2.45x10^{6}$
BETA	Impact-ionization parameter b_0	$V \bullet cm^{-1}$	0.0	$1.92x10^{6}$
LLDD	LDD region length (0 for no LDD)	m	0.0	$(0.05\text{-}0.2)x10^{-6}$
NLDS	LDD/LDS doping density (>$1x10^{19}$: D/S extensions)	cm^{-3}	$5.0x10^{19}$	$1x10^{19}$
GAMMA	BOX fringing field weighting factor	-	0.3	0.3-1.0

Table 4: UFSOI-4.5 FD MOSFET Model Parameters

KAPPA	BOX fringing field weighting factor	-	0.5	0.5-1.0
BGIDL	GIDL exponential factor (0 for no GIDL)	V•m^{-1}	0.0	(4-8)x10^{9}
JRO	Body-source/drain junction recombination current coefficient	A•m^{-1}	1.0x10^{-10}	10^{-11}-10^{-9}
M	Junction non-ideality factor	-	2.0	1.0-2.0
CGFDO	Gate-drain overlap capacitance	F•m^{-1}	0.0	1x10^{-10}
CGFSO	Gate-source overlap capacitance	F•m^{-1}	0.0	1x10^{-10}
CGFBO	Gate-body overlap capacitance	F•m^{-1}	0.0	0.0
RD	Specific drain parasitic resistance	Ω.m	0.0	(100-1000)x10^{-6}
RS	Specific source parasitic resistance	Ω.m	0.0	(100-1000)x10^{-6}
RHOB	Body sheet resistance	Ω/sq	0.0	30x10^{3}
DL	Channel-length reduction	m	0.0	(0.05-0.15)x10^{-6}
DW	Channel-width reduction	m	0.0	(0.1-0.5)x10^{-6}
LDIFF	Effective diffusion length in source/drain	m	0.1x10^{-6}	(0.1-0.5)x10^{-6}
SEFF	Effective recombination velocity in source/drain	cm•s^{-1}	10^{5}	(0.5-5)x10^{5}
FNK	Flicker noise coefficient (0 for no flicker noise)	F.A	0.0	0-10^{-25}
FNA	Flicker noise exponent	-	1.0	0.5-2
Flag Parameters				
Name	**Description**	**Units**	**Default**	**Typical Value**
BJT	Parasitic bipolar flag (0: off; 1: on)	-	1	1
TPG	Type of gate material (+1: opposite to body; -1: same as body)	-	+1	+1
TPS	Type of substrate material (+1: opposite to body; -1: same as body)	-	-1	-1

Table 4: UFSOI-4.5 FD MOSFET Model Parameters

SELFT	Self-heating flag (0: no self heating; 1: approximate model; 2: full model)	-	0	0
Optional Model Parameters				
Name	**Description**	**Units**	**Default**	**Typical Values**
TAUO	Carrier lifetime in lightly doped region	s	Calculated	10^{-7}-10^{-5}
VFBF	Front-gate flatband voltage	V	Calculated	-1 (nMOS) 1 (pMOS)
VFBB	Back-gate flatband voltage	V	Calculated	-
WKF	Front-gate work function difference	V	Calculated	**~ VFBF**
WKB	Back-gate work function difference	V	Calculated	-
BFACT	V_{DS}-averaging factor for mobility degradation	-	0.3	0.1-0.5
FVBJT	BJT current directional partioning factor (0 for lateral s1D flow)	-	0.0	0-1
RHOSD	Source/drain sheet resistance	Ω/sq	0.0	50

account for the 2-D fringing fields in the BOX, **GAMMA** and **KAPPA** must be properly evaluated. The initial values for **GAMMA** and **KAPPA**, based on **TOXB**, were extracted from 2-D MEDICI simulations [13]; they are given in Table 5. Since the UFSOI model assumes that the

Table 5: BOX Fringing-Field Parameters (Extracted from MEDICI)

TOXB (nm)	GAMMA	KAPPA
≤50	1.0	1.0
100	0.7	0.9
200	0.5	0.7
350	0.3	0.5

FD device is strongly fully depleted (except in accumulation), the parameters associated with floating-body effects, such as **ALPHA**, **BETA**, **TAUO**, **JRO**, **M**, **LDIFF**, and **SEFF**, are less important for most FD/SOI MOSFETs. Nonetheless, the transient bipolar effect in the FD/SOI MOSFET can be important in certain applications, for which the associated parameters must be tuned reliably; these parameters, **JRO**, **M**, **SEFF**, and **LDIFF**, can be evaluated from transient leakage-current measurements [3]. As for the NFD model, several of the parameters listed in Table 4 are either unimportant or inapplicable for this technology. For example, **NQFF** is typically low enough that it is not significant in a scaled technology, and **NQFB** is generally not critical relative to the charge defined by **NSB**. **NQFSW** can be set to 0 generally, unless narrow-width effects on threshold voltage are important, in which case measured data from a narrow-W device is needed for evaluation. We suggest that the impact-ionization parameters, **ALPHA** and **BETA**, be set to their default (physical) values of 2.45×10^6 /cm and 1.92×10^6 V/cm, respectively, for nMOS [10], [11], and adequately adjusted for pMOS. Also, **SEFF** could be tuned roughly to the BJT-induced drain-source breakdown voltage for high-voltage applications.

For the MIT Lincoln Lab technology [8], with dual-polysilicon gates (n^+ poly for nMOS and p^+ poly for pMOS), the parameters listed in Table 6 are evaluated directly, for both nMOS and

Table 6: Model Parameters Evaluated Directly from Technology Information

Parameter	Value
TOXF	8.0 nm
TOXB	185 μm
TB	50 nm
TPG	+1
TPS	-1, +1
W (drawn)	7 μm
L (drawn)	0.5 and 0.25 μm

pMOS devices. Now, only 14 key parameters, which are initially estimated as noted, need to be tuned: **NSB**, **NBODY**, **TB** (if necessary), **QM**, **NGATE**, **UO**, **THETA**, **VSAT**, **GAMMA**, **KAPPA**, **BGIDL**, **RD**, **RS**, and **DL**. Since the measured data we acquired do not include C-V characteristics, we do not tune **QM** and **NGATE** for this example. Actually, since the gate-oxide thickness of this technology is not very thin, these parameters are not really significant. In other cases, however, if the polysilicon gate-depletion and energy-quantization options are needed, we initially estimate **NGATE** to be $5.0\text{x}10^{-19}$ and **QM** to be 0.4, where the latter is based on a general calibration of the UFSOI model to numerically simulated devices with channel doping in the range 10^{16} - 10^{18} cm^{-3} [9]. The methodology for tuning **NGATE** and **QM** discussed in the NFD calibration is applicable here as well. If the noted options are not used, then **TOXF** is set to the measured electrical value of the oxide thickness, which is typically 10-20% thicker than the physical value. The overlap capacitances, **CGFDO** and **CGFSO**, can be calculated (= $\frac{\varepsilon_{ox}\mathbf{DL}}{2\mathbf{TOXF}}$, which neglects possible fringing) or can be tuned from a measured gate C-V characteristic. The other parameters are either unimportant or inapplicable for this technology. The tuning is done systematically as detailed in the following sections.

3.2. Long-L Calibration

Unlike the parameter evaluation for the NFD model, the FD model parameters can not always be tuned for long and short L sequentially because of the BOX fringing-field effect. If the subthreshold slope (S) increases abnormally as channel length is decreased or V_{DS} is increased, then the fringing fields are probably significant, and **GAMMA** and **KAPPA** must be tuned beyond the values in Table 5. In spite of this effect however, other parameters such as **DL**, **RD**, **RS**, and **VSAT** can still be evaluated according to their importance in short-L devices only. In this section, we will focus on the evaluations of **NSB**, **GAMMA**, **TB**, **NBODY**, **UO**, and **THETA**. Due to the limited availability of measured data, we choose the 0.5 μm device to demonstrate the long-L calibration, even though it is not long enough to be absolutely void of short-channel effects.

Stage 1

Evaluated Parameters	Measurement Data	Device
NSB, **GAMMA**, **TB**, **NBODY**	I_{DS} vs. V_{GfS} @ low V_{DS} (50 mV)	Long - L

In weak inversion, the diffusion of carriers throughout the "fully depleted" film body is accounted for in the UFSOI model by integrating the carrier charge across the entire film; "front" and "back" channels are thereby defined, and front and back channel-length modulation is accounted for as well [13]. The increased charge at the back surface will also reduce the front-channel threshold voltage through the charge-coupling effect [14]. Therefore both front- and back-gate surface charge can influence the subthreshold characteristic. However, since the front-gate oxide thickness is typically much thinner than back-gate oxide thickness, **NSF** tuning is usually not needed. We first check the subthreshold slope of the I_{DS}-V_{GfS} characteristic at low V_{DS} for the long-L device to determine the importance of **NSB**. If S is near ideal (~60mV), then **NSB** must be low, and hence we can skip its evaluation. In this example, S is found to be 64.4 and 64.3 mV for the nMOS and pMOS devices, respectively (>60mV because of the fringing field in the BOX), and so we do not evaluate **NSB** initially. We next tune **TB** and **NBODY** (and perhaps **NSB**) iteratively to fit the current and slope of the I_{DS}-V_{GfS} characteristic at low V_{DS} in weak inversion; **GAMMA** is initially estimated from Table 5. Results are illustrated in Fig. 14.

As part of the 2-D BOX fringing-field modeling, an effective back-gate bias is defined as [13]

$$V_{GbS(eff)} \equiv V_{GbS} + \frac{\mathbf{TOXB}^2}{L^2}(\mathbf{KAPPA} V_{DS} + \mathbf{GAMMA} E_0 L) \qquad (10)$$

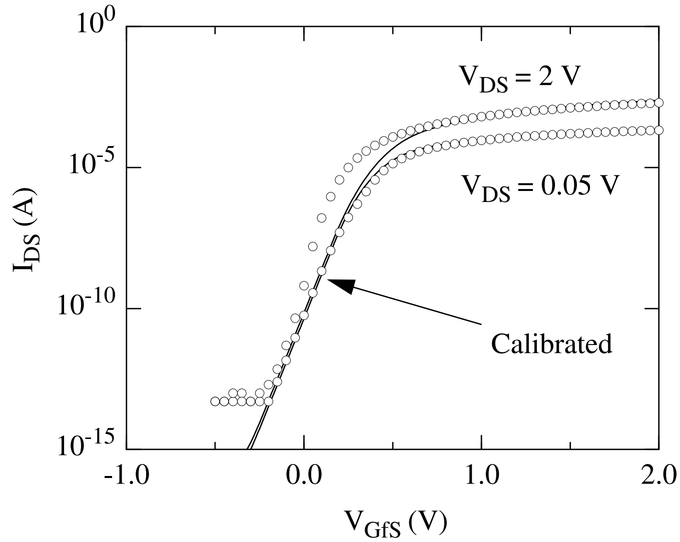


Fig. 14(a). I_{DS} -V_{GfS} characteristics of a 0.5 μm FD/SOI nMOS device (Stage 1).

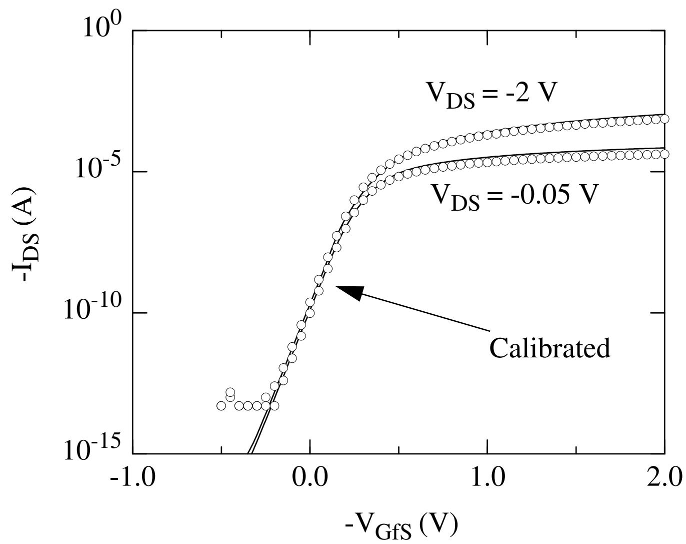


Fig. 14(b). I_{DS} -V_{GfS} characteristics of a 0.5 μm FD/SOI pMOS device (Stage 1).

where E_0 ($\equiv -\partial\Psi/\partial y|_{x\,=\,\mathbf{TB},\,y\,=\,0}$) represents the source of the fringing field; $V_{GbS(eff)}$ reduces to V_{GbS} for very long L and/or thin **TOXB**. As evident in (10) then, **GAMMA** and **KAPPA** can be evaluated with reference to their relative significance for different L's and V_{DS}'s; for example, **KAPPA** is more important for high V_{DS}, which will be discussed later. Since **TB** not only affects the slope but also affects the current magnitude (i.e., threshold voltage), an iterative yet uncomplicated scheme should be used in this stage. We thereby confirm **GAMMA** = 0.5 (given previously) and **TB** = 50 nm (consistent with technology) for both nMOS and pMOS, and we get **NBODY** = 2.2 x 10^{17} cm^{-3} and 2.0 x 10^{17} cm^{-3} for nMOS and pMOS, respectively.

Note in Fig. 14(a) the significant discrepancy at high V_{DS} for the nMOS device; a subthreshold kink is exhibited. We infer that it is mainly due to the device becoming NFD (when $V_{BS} > 0$, which tends to shrink the channel depletion region in a MOSFET). This characteristic stresses the fact that in order to develop a good FD/SOI MOSFET with reliable (and predictable) characteristics without floating-body effects, the body doping and film thickness must be carefully designed to ensure full depletion of the body over the entire range of anticipated bias.

An additional stage could be inserted here to evaluate **BGIDL** from the high-V_{DS} I_{DS}-V_{GfS} subthreshold characteristic included in Fig. 14. The evaluation would follow from simply fitting the GIDL current, usually seen for $V_{GfS} < 0$ for nMOS and $V_{GfS} > 0$ for pMOS. However, the characteristics we have for the FD/SOI technology do not show much GIDL current, and hence **BGIDL** is not evaluated.

<u>Stage 2</u> (optional with **TOXF** set to electrical gate-oxide thickness)

Evaluated Parameters	Measurement Data	Device
QM, **NGATE**	C_{GfS} vs. V_{GfS} @ low V_{DS} (~0 V)	Long-L

From the front-gate C-V characteristic, **QM** and **NGATE** can be tuned based on the estimation of capacitance lowering in strong inversion, respectively, as depicted in Fig. 3 for the NFD model calibration. Physically both poly depletion and energy quantization have influences on capacitances and currents, especially in the strong-inversion regime. Nonetheless energy quantization could be still important around threshold voltage, and hence can lower the subthreshold current and increase the threshold voltage. As a consequence, the calibration of subthreshold current demonstrated in Stage 1 might need refinement. In this example, C-V data are not available, and further **QM** and **NGATE** are not important. When they are, refer to the more detailed discussion of C-V calibration in Stage 3 of the NFD model calibration.

Stage 3

Evaluated Parameters	Measurement Data	Device
UO, **THETA**	I_{DS} vs. V_{GfS} @ low V_{DS} (50 mV)	Long-L

Similar to Stage 5 of the NFD model parameter tuning, **UO** and **THETA** can be tuned directly from the I_{DS}-V_{GfS} characteristic at low V_{DS}, as indicated in Fig. 15. However, this stage should be linked to the **RD/RS** evaluation in Stage 5, at least in this example, since the 0.5 μm device is not totally immune from **RD/RS** influence. For a longer-L device, e.g., L = 1 μm, **UO** and **THETA** could be tuned independent of **RD/RS**. In conjunction with Stage 5, we obtain **UO** = 700 $cm^2/V/s$ and **THETA** = 0.75 x 10^{-6} cm/V for nMOS, and **UO** = 200 $cm^2/V/s$ and **THETA** = 1.6 x 10^{-6} cm/V for pMOS.

3.3. Short-L Calibration

Now the tuning process continues with the short-L (target) device, beginning with the parameter set obtained from the long-L device tuning. In fact, if long-L device data are not

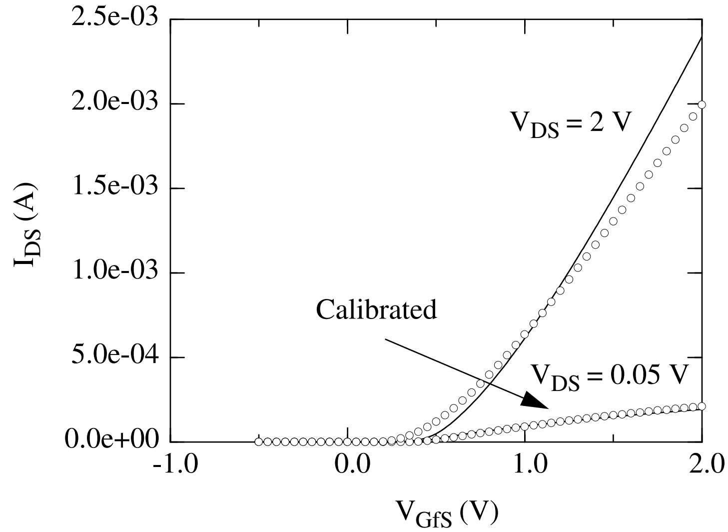


Fig. 15(a). I_{DS} -V_{GfS} characteristics of a 0.5 μm FD/SOI nMOS device (Stage 3).

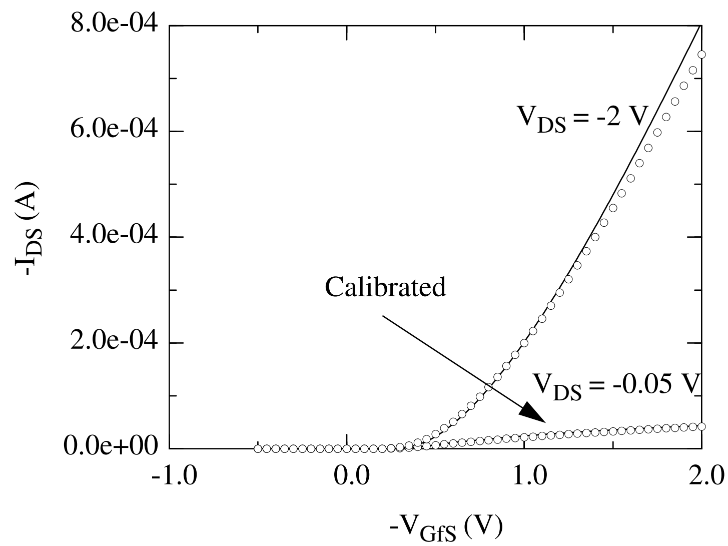


Fig. 15(b). I_{DS} -V_{GfS} characteristics of a 0.5 μm FD/SOI pMOS device (Stage 3).

available, the calibration could be done with only the short-L device data, albeit with a bit more complexity. As noted in the short-L calibration of the NFD model, self-heating is usually more prevalent in short-L device data, and must be carefully avoided to ensure the integrity of the parameter evaluation. (The UFSOI models do have a self-heating option [5], which uses two additional parameters (**RTH** and **CTH**) that could be tuned). The remaining parameters to be evaluated from the short-L device data are **DL**, **KAPPA**, **RD**, **RS**, and **VSAT**. We choose the target device with L = 0.25 μm for the short-L calibration.

Stage 4

Evaluated Parameters	Measurement Data	Device
DL, **KAPPA**	I_{DS} vs. V_{GfS} @ high (2 V) & low V_{DS} (50 mV)	Short-L

The channel-length reduction **DL** can be evaluated (refined) from its influence on the short-channel effects. For example, in the subthreshold region, the DIBL effect is worsened as **DL** increases. However, as described in (10), **KAPPA** tends to be predominant for high V_{DS} and short L. So, to account for both the fringing-field and the short-L effects, we tune (refine) **DL** and **KAPPA** simultaneously by fitting the current and slope of subthreshold I_{DS}-V_{GfS} characteristics at different values of V_{DS}, as illustrated in Fig. 16. Unexpectedly, we find that **KAPPA** for the nMOS device needs to be increased significantly from the value in Table 6 to match the abnormally high subthreshold current at high V_{DS}. Although the BOX field-fringing could be the underlying reason for the high current, this result portends the possibility of punchthrough or, as was evident for the long-L device, a drain-induced transition to the NFD mode, which would result in a higher S (see (1)) as in Fig. 16(a). Nonetheless, we obtain **DL** = 0.06 μm and **KAPPA** = 1.0 for nMOS, and **DL** = 0.018 μm and **KAPPA** = 0.7 (given previously) for pMOS.

Stage 5

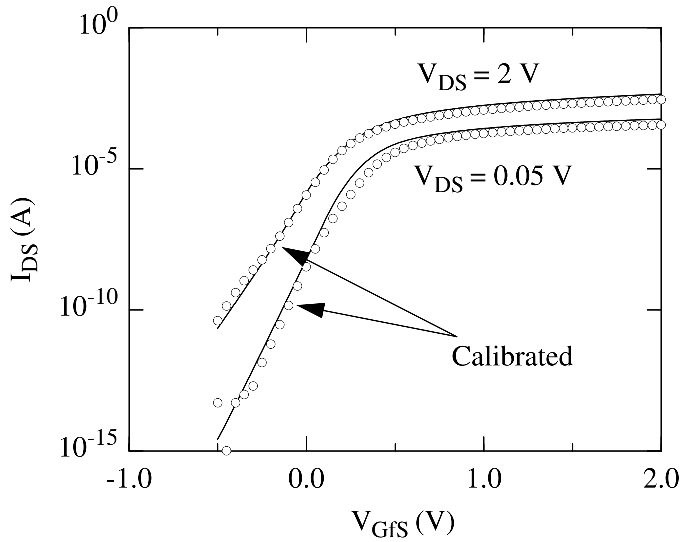


Fig. 16(a). I_{DS} -V_{GfS} characteristics of a 0.25 μm FD/SOI nMOS device (Stage 3).

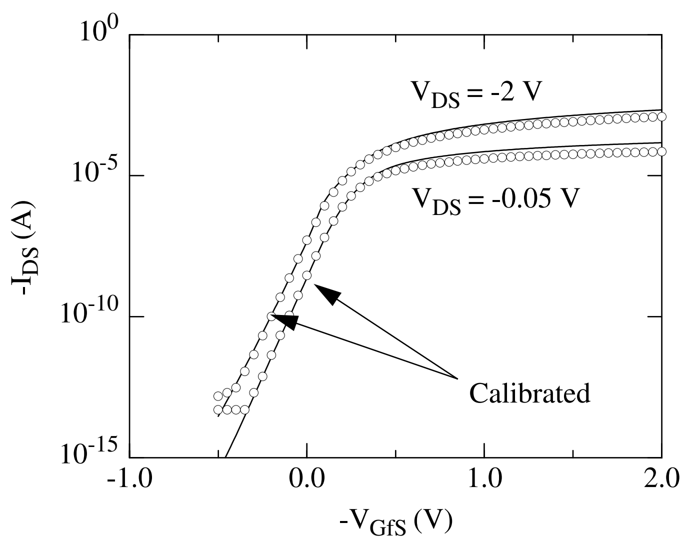


Fig. 16(b). I_{DS} -V_{GfS} characteristics of a 0.25 μm FD/SOI pMOS device (Stage 3).

Evaluated Parameters	Measurement Data	Device
RD, **RS**	I_{DS} vs. V_{GfS} @ low V_{DS} (50 mV)	Short-L

Fig. 17 shows that **RD** and **RS** can be evaluated from the linear region of the I_{DS} -V_{GfS} characteristics. Since **RS/RD** could have been of some importance in the "long-L" device, **UO** and **THETA** should be fine-tuned here to sustain the agreement with the long-L data, unless the channel length is so long that **RS/RD** will not cause any noticeable effect. Assuming **RS = RD** due to device symmetry, we tune **RS/RD** to 200 x 10^{-6} Ω-m for nMOS and 900 x 10^{-6} Ω-m for pMOS.

<u>Stage 6</u>

Evaluated Parameter	Measurement Data	Device
VSAT	I_{DS} vs. V_{DS} @ low power region	Short-L

As shown in Fig. 18, we tune **VSAT** from the I_{DS}-V_{DS} characteristics at high V_{GfS} with V_{DS} ~ V_{DS}(sat), where the saturation is governed by velocity saturation and not pinch-off. Note that self-heating can and must be avoided; it is apparent in the nMOS device at higher V_{DS} where the DC power dissipation is larger. We tune **VSAT** to be 0.65 x 10^7 cm/s for nMOS and 0.45 x 10^7 cm/s for pMOS.

3.3 Verification

Due to the thinner body of the FD/SOI MOSFET, which implies higher thermal resistance, the self-heating phenomenon, discussed in Section 2.4, may be more severe than in the NFD/SOI device. However, the characteristics showing the final calibration of the FD model to the MIT Lincoln Lab CMOS technology, plotted in Figs. 19 and 20, do not cover very high-power regions; only the measured nMOS characteristics for V_{DS} and V_{GfS} near 2 V reflect any self-

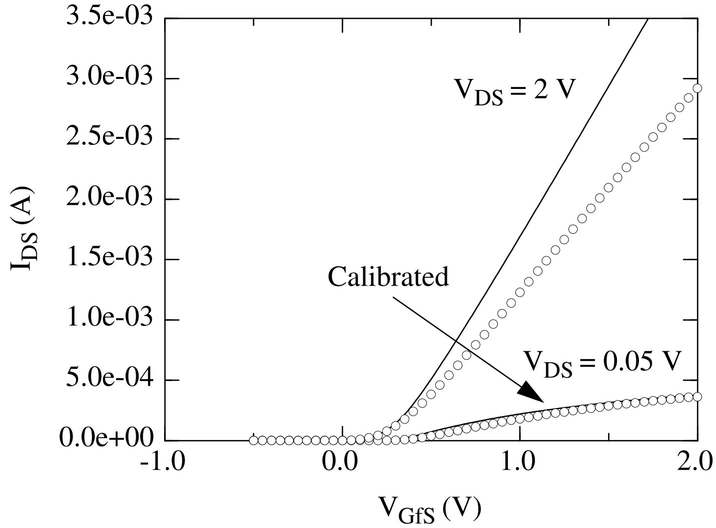


Fig. 17(a). I_{DS} -V_{GfS} characteristics of a 0.25 μm FD/SOI nMOS device (Stage 5).

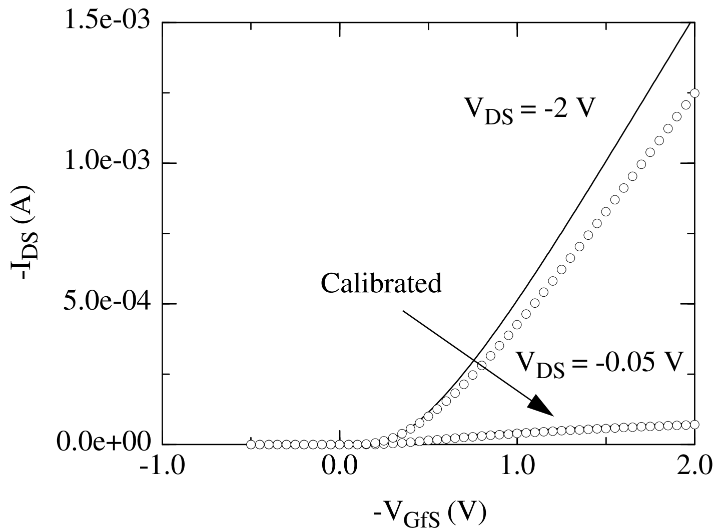


Fig. 17(a). I_{DS} -V_{GfS} characteristics of a 0.25 μm FD/SOI pMOS device (Stage 5).

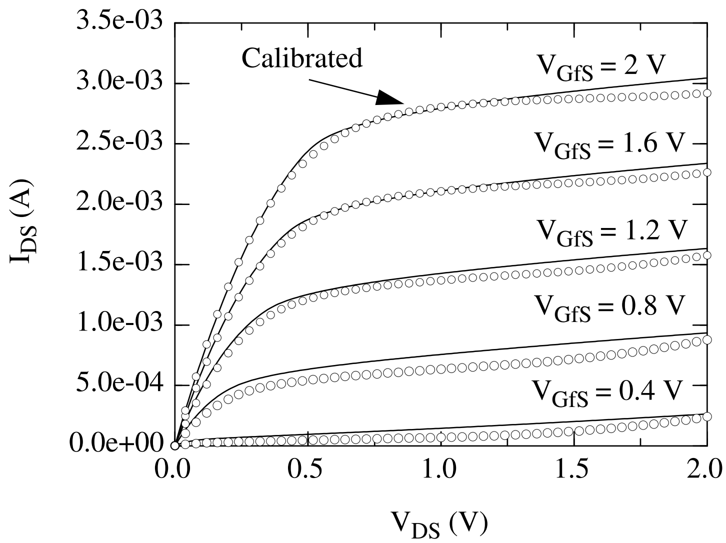


Fig. 18(a). I_{DS} -V_{DS} characteristics of a 0.25 μm FD/SOI nMOS device (Stage 6).

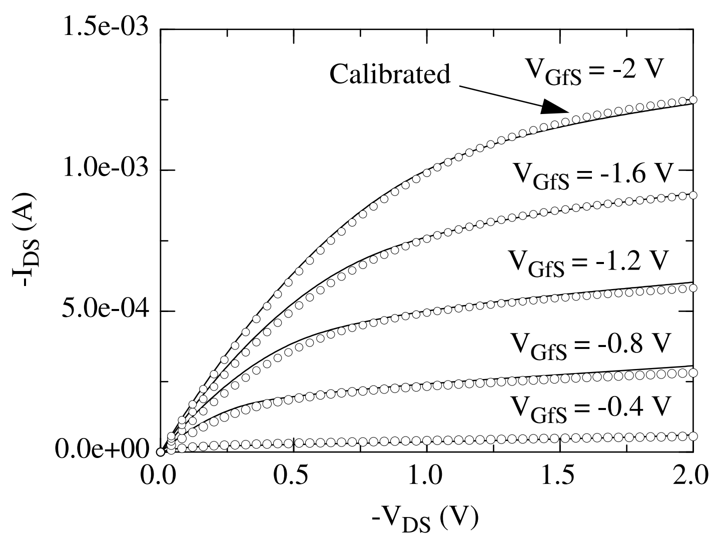
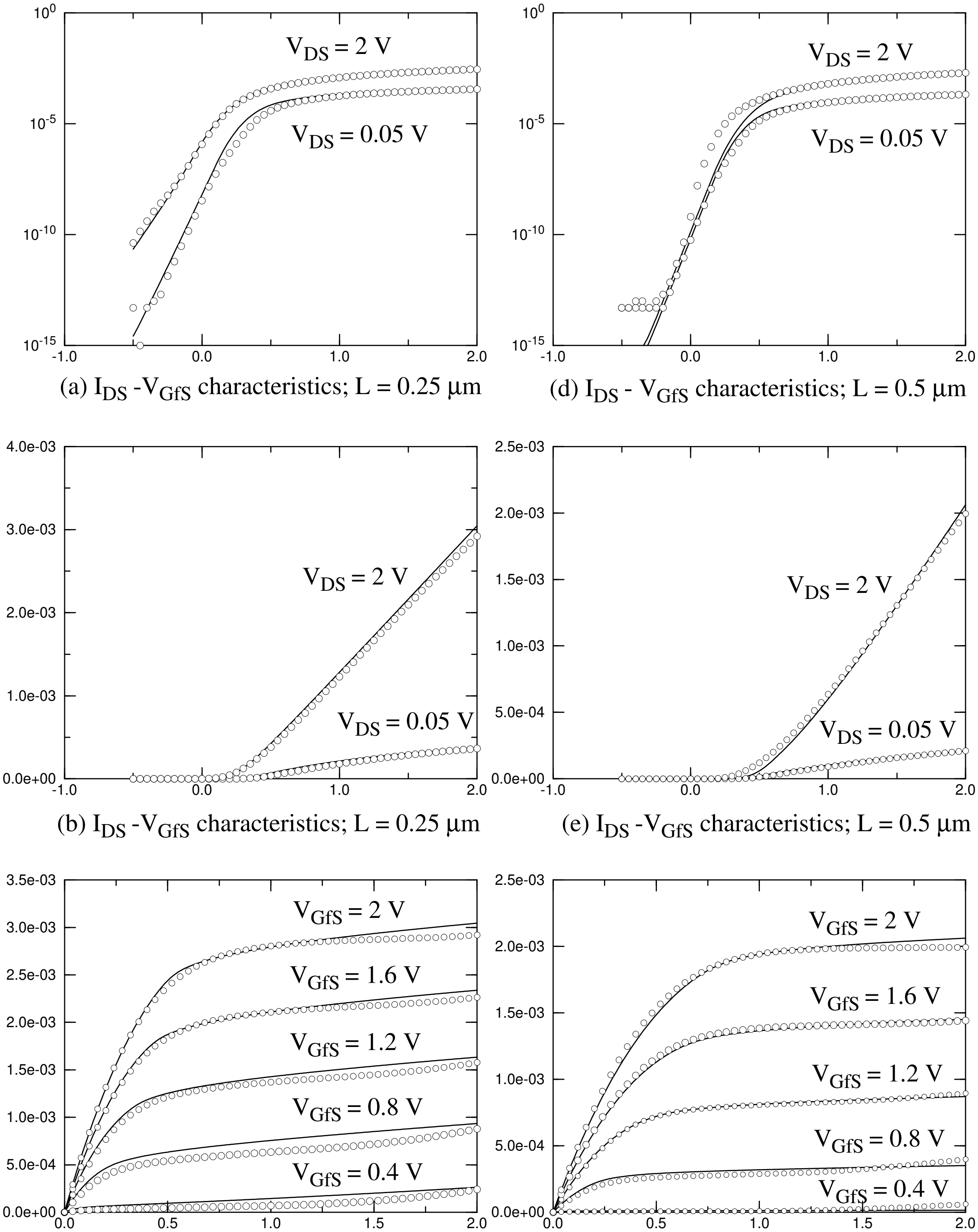


Fig. 18(a). I_{DS} -V_{DS} characteristics of a 0.25 μm FD/SOI pMOS device (Stage 6).



(a) I_{DS} -V_{GfS} characteristics; L = 0.25 μm

(d) I_{DS} - V_{GfS} characteristics; L = 0.5 μm

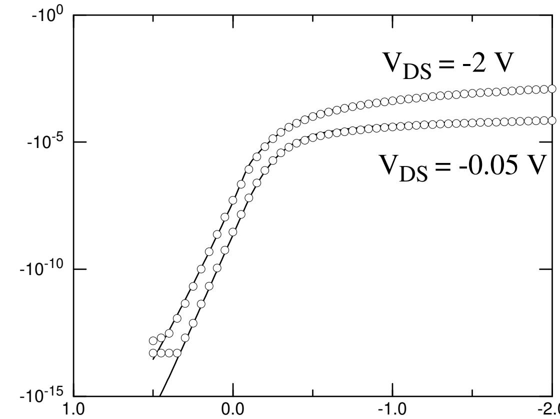
(b) I_{DS} -V_{GfS} characteristics; L = 0.25 μm

(e) I_{DS} -V_{GfS} characteristics; L = 0.5 μm

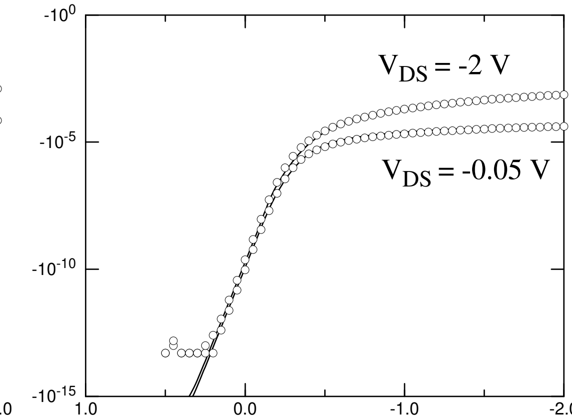
(c) I_{DS} -V_{DS} characteristics; L = 0.25 μm

(f) I_{DS} -V_{DS} characteristics; L = 0.5 μm

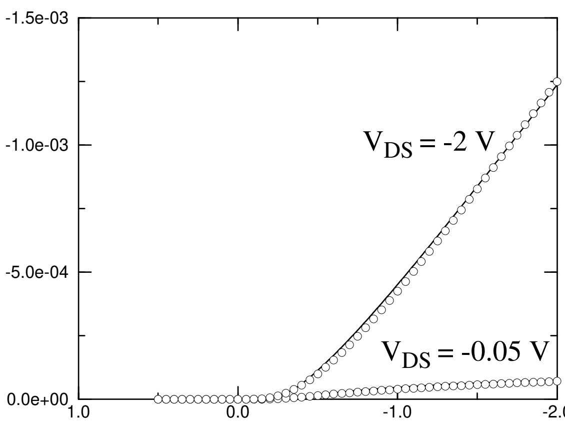
Fig. 19. Calibrated I(A) - V(V) characteristics of FD/SOI nMOS devices.



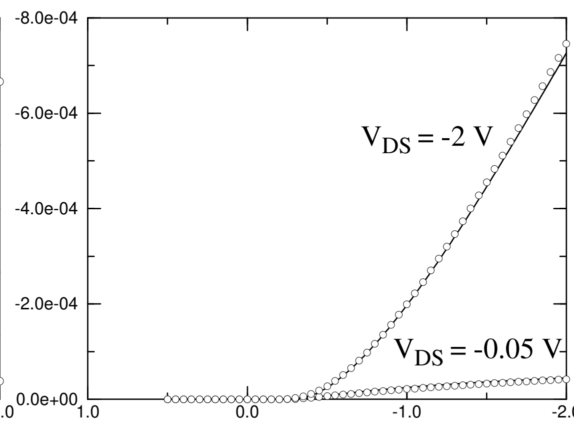
(a) I_{DS} -V_{GfS} characteristics; L = 0.25 μm



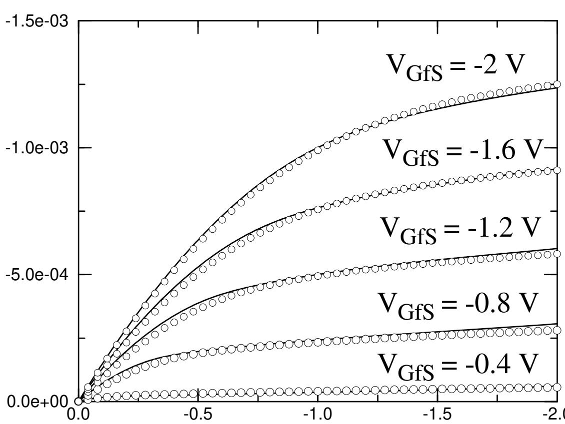
(d) I_{DS} - V_{GfS} characteristics; L = 0.5 μm



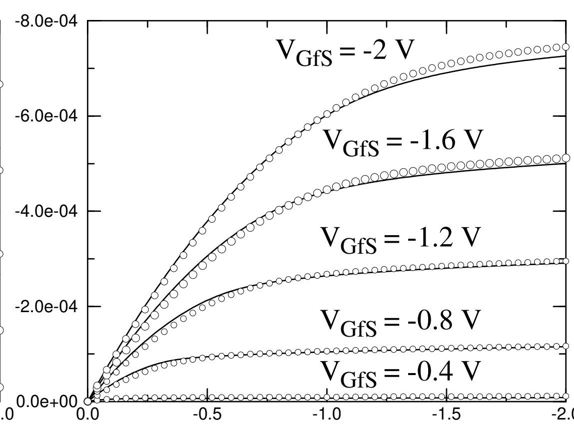
(b) I_{DS} -V_{GfS} characteristics; L = 0.25 μm



(e) I_{DS} -V_{GfS} characteristics; L = 0.5 μm



(c) I_{DS} -V_{DS} characteristics; L = 0.25 μm



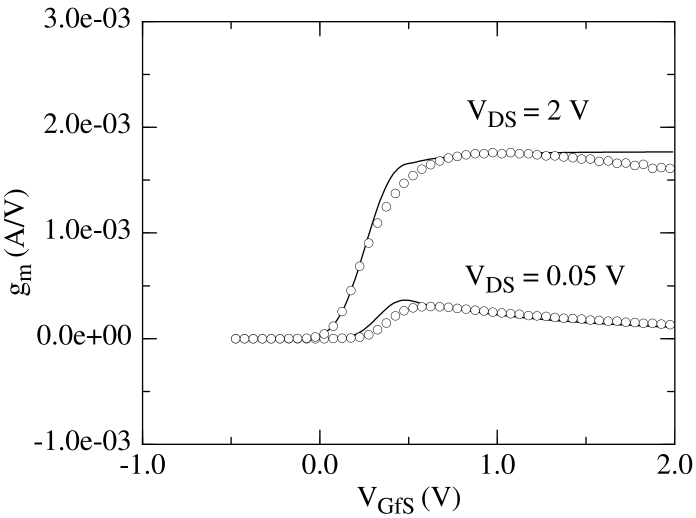
(f) I_{DS} -V_{DS} characteristics; L = 0.5 μm

Fig. 20. Calibrated I(A) - V(V) characteristics of FD/SOI pMOS devices.

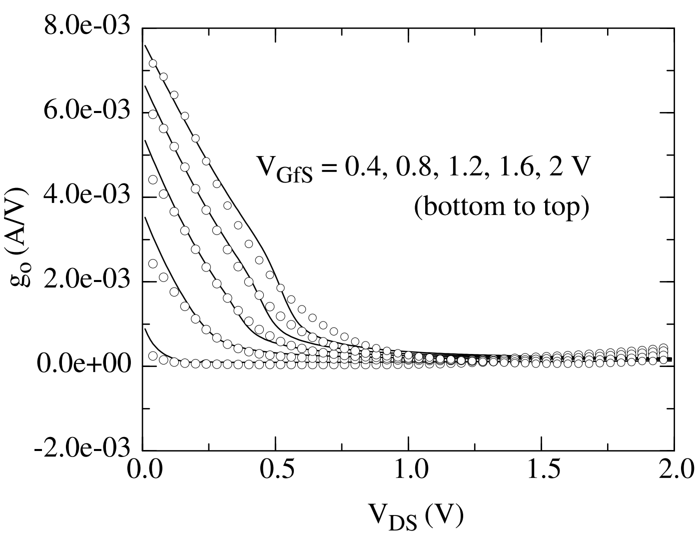
heating. The FD model (without self-heating) calibration is very good, except where the nMOS devices possibly become NFD as noted previously. Figures 21 and 22 show corresponding simulated and measured conductances, with very good agreement as well. The nMOS and pMOS model parameters derived for the target channel length are listed in Table 7. Unlisted parameters, which are unimportant, are set to their default values.

Table 7: Evaluated Parameters for MIT Lincoln Lab's 0.25μm FD/SOI CMOS Devices

Parameters	nMOS	pMOS
TOXF	8.0 nm	8.0 nm
TOXB	0.185 μm	0.185 μm
TB	0.05 μm	0.05 μm
NBODY	2.2×10^{17} cm^{-3}	2.0×10^{17} cm^{-3}
UO	700. cm^{2}/V/s	200. cm^{2}/V/s
THETA	0.75×10^{-6} cm/V	1.6×10^{-6} cm/V
VSAT	0.65×10^{7} cm/s	0.45×10^{7} cm/s
KAPPA	1.0	0.7
GAMMA	0.5	0.5
TPG	1	1
TPS	-1	1
RD	$200. \times 10^{-6}$ Ω-m	$900. \times 10^{-6}$ Ω-m
RS	$200. \times 10^{-6}$ Ω-m	$900. \times 10^{-6}$ Ω-m
DL	0.06 μm	0.018 μm

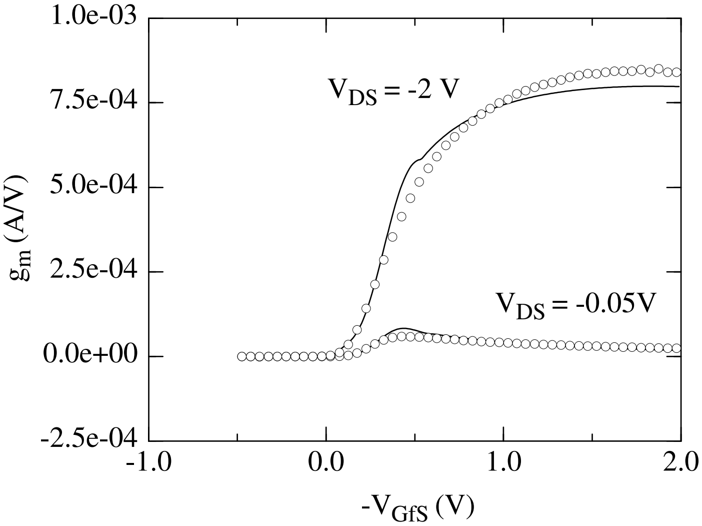


(a) Transconductance; L = 0.25 μm

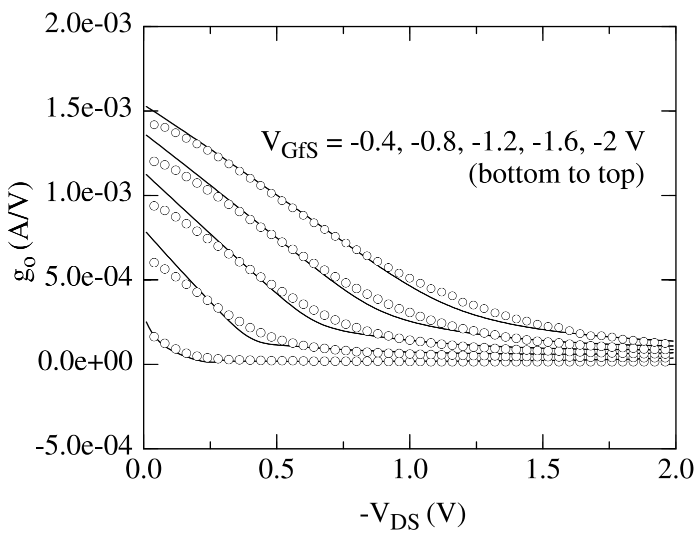


(b) Output conductance; L = 0.25 μm

Fig. 21. Calibrated conductances of FD/SOI nMOS device.



(a) Transconductance; L = 0.25 μm



(b) Output conductance; L = 0.25 μm

Fig. 22. Calibrated conductances of FD/SOI pMOS device.

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