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A Unified Process-Based Compact Model for Scaled PD/SOI and Bulk-Si MOSFETs

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ABSTRACT

A process/physics-based compact model (UFPDB), unified for PD/SOI and bulk-Si MOSFETs with a single small set of parameters, is overviewed. The utility of UFPDB, e.g., for benchmarking PD/SOI and bulk-Si CMOS and for projecting performances of scaled technologies, is demonstrated via UFPDB/Spice3 device/circuit simulations.

Keywords: Physical compact model, predictive circuit simulation, Si MOSFETs, scaled CMOS.

1. INTRODUCTION

As CMOS technologies are being scaled to extremely short gate lengths (~10nm at the end of the SIA roadmap [1]), it is becoming apparent that conventional, largely empirical compact modeling of MOSFETs for circuit simulation will be inadequate [2]. The physics underlying such scaled MOSFETs (e.g., the quantum mechanics of carrier confinement and the near-ballistic transport of heated carriers) is quite complex, which implies the need for truly physical compact modeling that does not depend on complicated measurement-based optimization, or extraction, of large numbers of model parameters [3].

The BSIM model [3], [4] is currently the most widely used model for CMOS circuit simulation. It has evolved as technologies have been scaled, resulting in an empirical model having a prodigious number of parameters [2] that require copious amounts of measured data for extraction [3]. Such evolution, which is widening the gap between device and circuit simulation, portends limits to its utility for extremely scaled technologies. We offer in this paper a novel alternative to such evolutionary modeling: revolutionary fabrication *process-based* modeling, which, as we demonstrate, can yield a compact MOSFET model that is truly physical, amenable to simple parameter evaluation based on (process-defined) device structure, and hence predictive in nature. Such modeling, which effects a useful tradeoff between the computational intensiveness of numerical device simulation and the empiricism of conventional modeling for circuit simulation, is useful for IC TCAD and scaled CMOS performance projections, as well as circuit design.

The process-based model we describe, UFPDB [5], is unified for application to partially depleted (PD) SOI as well as bulk-Si MOSFETs, with only one small set of parameters that can be evaluated mainly from knowledge of the device structure and well known material (i.e., Si, SiGe, SiO_2, etc.) properties. We exemplify the physics-based nature of UFPDB by describing its accountings for impact ionization and carrier velocity overshoot, both of which are based on the carrier energy-balance equation. We demonstrate unique utility of UFPDB by using it to benchmark projected performances of scaled PD/SOI and bulk-Si CMOS, which suggests a sustained advantage for the former as the devices are scaled to their limit (near the 70nm node of the SIA roadmap [1]).

2. THE UFPDB MODEL

The original version of UFPDB, i.e., UFSOI/NFD [6], was a model for only PD/SOI MOSFETs. It was developed [7] and evolved [8] - [12] with a main goal being to reliably simulate and predict floating-body (FB) effects [13] in PD/SOI CMOS devices and circuits. Thus, in addition to the intrinsic MOSFET modeling, which is based on a presumed retrograded, or super-haloed, channel, the model physically accounts for the parasitic lateral BJT [8], and carrier generation and recombination currents that can charge/discharge the floating body/base. The latter currents include source/drain junction tunneling [11] as well as thermal components, GIDL/GISL [11], and impact ionization [8], [14]. Further, the model is charge-based to ensure charge conservation and proper accounting for all transcapacitances [9], which define the fast-transient floating-body charging/discharging [13]. To allow truly physical modeling of the intrinsic MOSFET, the formalisms for weak ($V_{GfS} < V_{TW}$) and strong ($V_{GfS} > V_{TS}$) inversion are separated, with moderate-inversion channel current and terminal charges, and their voltage-derivatives, being continuously defined by cubic spline functions based on solutions at the bias-dependent boundaries V_{TW} and V_{TS} [6], [7]. The formalisms, involving Newton-like iterative solutions of physics-based nonlinear equations, include accountings for polysilicon-gate depletion [12], carrier-energy quantization [12], and carrier velocity saturation with possible overshoot [15]. Currently, gate-body tunneling current, including indirect valence band-conduction band components which depend on bandgap narrowing as well as the quantization in the channel, is being added to UFPDB so that FB effects in extremely scaled devices with ultra-thin oxides are completely accounted for. The process/physics basis of the model enabled direct implementation of the temperature dependences [10], [16], including accounting for self-heating, without having to add any new parameters, and of the noise modeling [10] as well.

The network representation of the five-terminal UFPDB model (without gate tunneling) is shown in Fig. 1. The current and charge modeling, for the parasitic BJT as well as the intrinsic MOSFET, is physically coupled. The terminal (i = D,

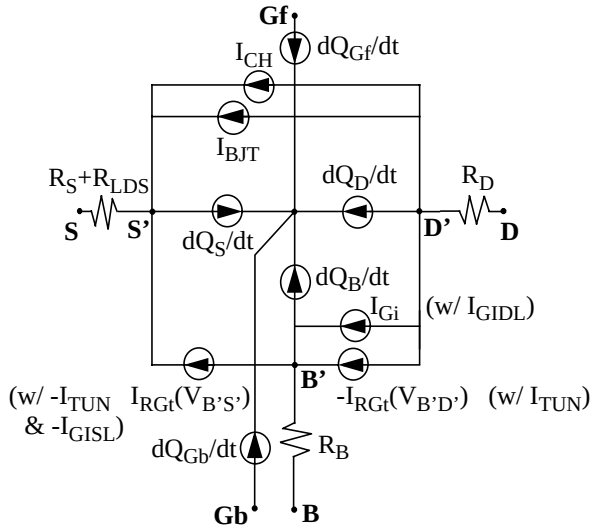

Fig. 1. Network representation of the UFPDB model.

S, Gf, Gb, B) charging currents [9] are defined based on the quasi-static approximation:

$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i}{\partial V_{jS}} \frac{dV_{jS}}{dt} , \qquad (1)$$

which, for scaled devices, nicely accounts for all transcapacitances and their influences on transient FB effects; j = D, Gf, Gb, and B. Note the intrinsic body (B') nodal equation, which can be symbolically expressed as

$$I_G - I_R = \frac{dQ_B}{dt} \qquad (2)$$

where Q_B is the body charge (that is supported by the body terminal) [9], which is linked to the other terminal charges via neutrality as indicated in Fig. 1, and I_G and I_R represent all the carrier generation and recombination currents linked to the body as shown in Fig. 1. Equations (1) and (2), with the underlying physics-based modeling for currents and charges, faithfully predict the FB (dynamic threshold-voltage (V_t) and/or BJT) effects, including the hysteresis [7], [13] due to the slow generation/recombination currents superimposed on the fast dQ_B/dt transients driven by the (trans)capacitive coupling of the body to the other terminals.

Because of the process basis, the number of UFPDB model parameters is small relative to those of empirical compact models [2], and the parameters can be evaluated straightforwardly [12], in contrast to the complex measurement-based extraction of empirical parameters [3]. The UFPDB parameters relate directly to device structure and/or physics, and hence even limited knowledge of the device structure can be used to define a reasonable "first-guess" model card; the first guess can in fact render the model predictive in some applications, e.g., performance projections of next-generation technologies as we demonstrate in Sec. 3. Otherwise, minimal measurement-based tuning of a few (~10) of the parameters completes the UFPDB calibration [12].

The UFPDB model formalism was unified for application to bulk-Si as well as PD/SOI MOSFETs without having to add any new model parameters [17]. This feature, enabled by the process basis of the model, allows direct performance comparisons of the two mainstream CMOS technologies without ambiguities in device structures. The bulk-Si option is activated by setting a flag parameter (BODY=2), which internally ties the substrate (Gb) to the body (B) and sets the back-gate (Gb) oxide thickness (TOXB) to near-zero, and by updating the substrate doping density (NSUB) to reflect the bulk-Si well doping. The areal component of the source/drain junction capacitance is thus physically modeled by the accounting for the MOS depletion charge in the substrate under the source/drain region [17].

The unified feature of UFPDB is reflected in Fig. 2 where predicted current-voltage characteristics of 70nm FB PD/SOI and bulk-Si MOSFETs are shown. The same set of model parameters, except for NSUB as noted above, was used for both devices. Note the higher currents and the current kinks in the PD/SOI characteristics, which result from FB effects due to forward $V_{B'S'}$ [18] as reflected by the DC version of (2).

Due to the physical modeling, and the need for the noted iterative solutions and moderate-inversion spline interpolations, circuit run-times with UFPDB are longer than those with empirical models. However, because we use approximate analytical derivatives for the Newton-Raphson nodal analysis, the times are not excessive. Comparison results vary, depending on model cards and circuits, but a recent UFPDB-BSIM3/SOI [3] (in Hspice) benchmark [19] showed UFPDB run-times to be only about 25% longer for transient simulations and less than 2-times longer for DC simulations.

To exemplify the truly physical nature of the UFPDB model, we overview the modeling of two mechanisms that are most significant in extremely scaled MOSFETs: impact-ionization current (I_{Gi} in Fig. 1) [14], a main driver of (DC and transient) FB effects, and velocity overshoot ($v_{sat(eff)}$ in I_{CH} in Fig. 1) [15], which reflects quasi-ballistic transport.

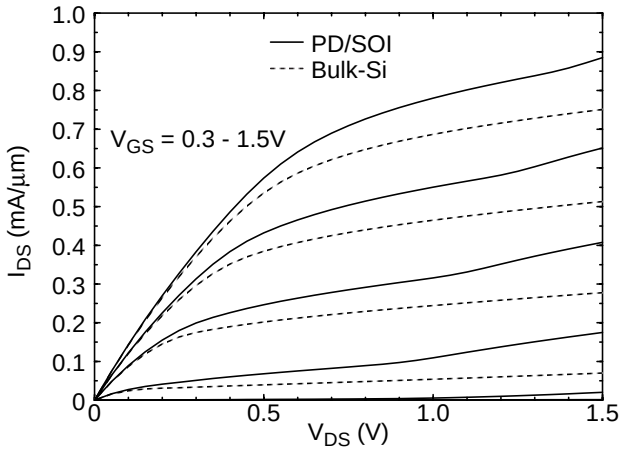

Fig. 2. UFPDB-predicted current-voltage characteristics of L_{eff}=70nm FB PD/SOI and bulk-Si nMOSFETs.

The basis for the modeling of both mechanisms is a simplified form of the energy-balance equation (i.e., the second-order moment of the Boltzmann transport equation):

$$\frac{d}{dy}(T_c(y) - T) + \frac{(T_c(y) - T)}{(5v\tau_w/3)} = \frac{2qE_y(y)}{5k_B} \qquad (3)$$

where T_c is the carrier temperature (defined by the kinetic energy which defines the impact-ionization rate α and the carrier mobility μ), E_y is the electric field along the channel, and τ_w is the energy-relaxation time. When $E_y(y)$ is high with steep gradients, as in scaled MOSFETs, (3) depicts how $T_c(y)$ lags $E_y(y)$, and thus reflects why local-field models for α and μ (which are used in empirical compact models) do not physically capture the device-structure dependences of impact ionization and hot-carrier transport. In the UFPDB I_{Gi} model [14], $E_y(y)$, defined from in the modeling of I_{CH} [7], is used in (3) to describe $T_c(y)$. Then, the uniform field-dependent (Chenoweth) $\alpha(E_y)$ is transformed into $\alpha(T_c)$ via a quasi-steady-state approximation by which $E_y(T_c)$ is given by (3) with the dT_c/dy term set to zero and the carrier velocity v assumed to be v_{sat}. In the UFPDB $v_{sat(eff)}$ model [15], (3) is combined with an expression for v derived from a simplified momentum-balance equation (i.e., the first-order moment of the Boltzmann transport equation), and the noted quasi-steady-state approximation, without the $v \cong v_{sat}$ assumption, is used to characterize $v[T_c(E_y)]$. With $E_y(y)$ known, the bias-dependent $v_{sat(eff)} > v_{sat}$, which replaces v_{sat} in the I_{CH} model, is then defined by v evaluated at the drain end of the channel.

Both of these T_c-dependent models in UFPDB have been shown to be reliable. The DC kink effect seen in Fig. 2 is driven by $I_{Gi}(T_c)$, as is premature drain-source breakdown at higher V_{DS} due to the parasitic BJT [8]. These FB effects, as predicted by UFPDB, are in good accord with device measurements [18]. Transient FB effects influenced by $I_{Gi}(T_c)$, e.g., hysteresis [13], [17], will be noted in Sec. 3. Higher on-state current (I_{on}) due to $v_{sat(eff)}(T_c)$ in scaled devices is exemplified in Fig. 3 where UFPDB-predicted current-voltage characteristics, with and without the overshoot option, for the bulk-Si nMOSFET in Fig. 2 are plotted. For this 70nm-channel device, the velocity overshoot results in almost 25% enhancement of I_{on} (at V_{DD} = 1.2V). This result, in accord with measured data [15], is physically consistent with the more rigorous scattering theory for quasi-ballistic transport in [20], whereas without the overshoot modeling there is absolute inconsistency.

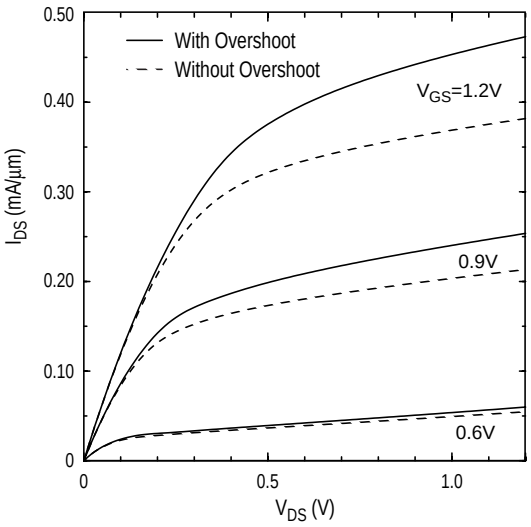

Fig. 3. UFPDB-predicted current-voltage characteristics of the L_{eff}=70nm bulk-Si nMOSFET with and without velocity overshoot.

3. UFPDB APPLICATION

To demonstrate the utility of the unified UFPDB model, we overview its use (in Spice3 [5]) in checking the performance advantage of FB PD/SOI CMOS relative to the bulk-Si counterpart, and in particular whether the advantage can be maintained as the technologies are scaled. The analysis [17] began with device and inverter-based ring-oscillator (RO) simulations for a contemporary 145nm-channel CMOS technology at V_{DD} = 1.8V. With controlled off-state currents (I_{off}), necessitating higher V_t for the PD/SOI devices (modeled via higher channel doping, i.e., UFPDB parameter NBL) because of FB effects [21], the predicted (dynamic steady-state) RO delay is 23% shorter for PD/SOI CMOS, in accord with actual speeds achieved. A dynamic-loading effect, defined by FB charging/discharging due to capacitive coupling, was shown to be the main reason for the SOI speed advantage [17].

Via UFPDB simulations, the two CMOS technologies were then physically scaled to 70nm channel lengths, with V_{DD} = 1.2V [17]. Such scaling, which was done in accord with the SIA roadmap [1], is possible with UFPDB because of its process basis; the new model parameters are defined directly based on the scaled device structures. Predicted current-voltage characteristics for the minimum-channel length (L_{min} = 50nm) PD/SOI and bulk-Si CMOS devices are shown in Fig. 4. For the FB SOI devices, characteristics with and without the V_t increase for I_{off} control are included. Note that even with such control, the SOI devices still have about a 10% I_{on} advantage.

However, the speed advantage of the PD/SOI CMOS is undermined by the scaling, as indicated by the predicted RO delays (at T = 27^{o}C) given in Table 1; the original 23% speed advantage is reduced to only 6.5%, again in accord with experimental results [21]. The simulations reveal that this loss of advantage is due mainly to the lower V_{DD}, which reduces the noted FB dynamic-loading effect. A dynamic kink effect, driven by $I_{Gi}(t)$, is now the primary FB effect, giving the reduced SOI advantage, and increased hysteresis as well.

Additional UFPDB-aided simulations [17] reveal, however, that the FB PD/SOI performance advantage will, in

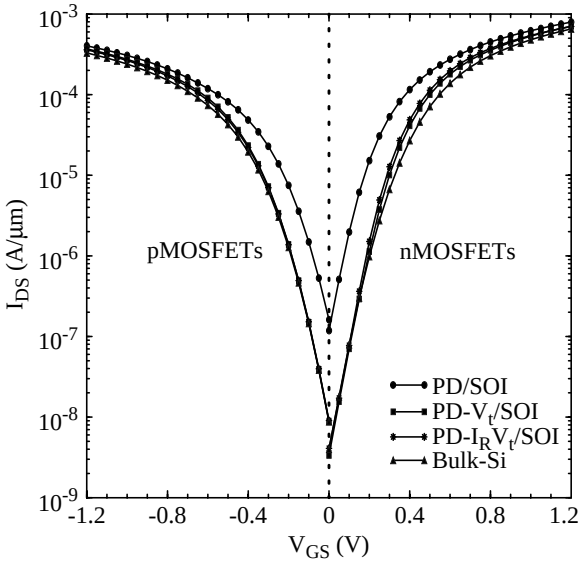

Fig. 4. UFPDB-predicted current-voltage characteristics of the L_{min}=50nm devices in the scaled L_{eff}=70nm PD/SOI and bulk-Si CMOS technologies; T = 27°C. The PD-V_t/SOI and PD-$I_R V_t$/SOI curves are, respectively, for the FB V_t-adjusted devices and hypothetical ones with higher (x10) I_R in (2).

actuality, remain significant (>10%) in the 70nm-channel length technology, and probably until the scaling limit of PD/SOI and bulk-Si MOSFETs (near the 70nm node of the SIA roadmap [1]) is reached. Two reasons for the sustained advantage are 1) real circuit operating temperatures are higher than room temperature; and 2) stacked logic gates (e.g., NAND circuits) are prevalent in real systems. With regard to 1), UFPDB inverter-based RO simulations at T = 85°C, contrasted with those at room temperature in Table 1, predict a 9.9% delay benefit for FB PD/SOI relative to bulk-Si. This enhancement results because less V_t increase is needed to control I_{off} due to the higher I_R in (2) at elevated temperatures [18]. Further, the predicted hysteresis (relative change in delay from the initial value to the dynamic steady-state value) is reduced from 11% at room temperature to 4.8% at the elevated temperature [17]. With regard to 2), UFPDB simulations of two-way NAND-based ROs show how the FB effects tend to offset the detrimental traditional body effect (reverse $V_{B'S'}$) in the stacked nMOSFETs, giving a speed benefit of >10% even at T = 27°C [17].

4. SUMMARY

The process/physics-based UFPDB compact model, unified for PD/SOI and bulk-Si MOSFETs, has been overviewed. Its truly physical nature was exemplified, and the afforded straightforward evaluation of its single small set of parameters, based on device structure, was discussed. Its predictive capability was demonstrated via UFPDB/Spice3 simulations that benchmarked scaled PD/SOI and bulk-Si CMOS technologies, projecting a sustained performance advantage for the former as the devices are scaled to their limit (near the 70nm node of the SIA roadmap [1]).

Table 1: UFPDB/Spice3-Predicted CMOS Inverter-Based Dynamic Steady-State RO Delays at Room and Typical Operating Temperatures for the L_{eff}=70nm PD/SOI (With and Without V_t Adjust for I_{off} Control) and Bulk-Si Technologies.

T	PD/SOI	PD-V_t/SOI	Bulk-Si
27°C	22.4ps	28.9ps	30.9ps
85°C	25.1ps	28.1ps	31.2ps

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