# Chapter 1

# Southampton Thermal Analogue SOI MOSFET Model User Guide

## 1.1 Introduction

This appendix presents a user guide for the Southampton Thermal AnaloGue (STAG) model version 2.5. STAG is a compact model for partially depleted SOI MOSFETs, implemented in version 3f5 of the Berkeley SPICE circuit simulator. The STAG model has been designed specifically for the reliable simulation of analogue SOI CMOS circuits and includes a rigorous physical treatment of self-heating and floating body effects. Particular emphasis has been placed on numerical robustness to prevent convergence problems during the simulation of high-gain analogue circuits. The resulting model uses a surface potential based single-piece formulation with continuous derivatives in all regions of device operation. The STAG model is charge conserving and includes static, transient, small-signal and noise models. A 'thermal' node is provided to allow simulation of thermal coupling between devices.

## 1.2 New Features in STAG v2.5

A number of changes have been made to STAG in version 2.5, many of which are intended to improve the usability of the model for practical circuit design. The changes all pertain to the STAG auxiliary model, and leave the core model of v2.1 unchanged.

### 1.2.1 Thermal Self-Heating

STAG v2.5 has the capacity to model up to five thermal nodes in the electro-thermal equivalent circuit. Each of these nodes corresponds to an individual thermal time constant, which appears as a pole-zero doublet on a frequency response plot. The thermal resistances, RT0-4, and thermal capacitances, CT0-4, are device instance parameters. RT0 and CT0 are the first order thermal parameters, and are shortened to RT and CT in the

STAG model. We will consider RT1-4 and CT1-4 later; for now we will concentrate on the way that RT and CT are handled. The key point to remember about STAG v2.5 is that the first order self-heating model is switched *on* by default; if RT and CT are not specified by the user, STAG will calculate them using a simple physical model.

**First Order Self-Heating Model**

There are several regimes by which RT and CT can be specified for any given device in STAG. The following list gives the priorities of these different regimes:

1. By directly specifying RT and/or CT, the user overrides all other priorities.

2. If are RT and CT are not specified, the user can set RTA and CTA, which are the area scaling factors for the thermal resistance and thermal capacitance. RTA and CTA are model parameters; if assigned values in the model netlist, they are used to calculate RT and CT for all devices in a circuit using the following relations:

$$CT = CTA \cdot A_T \tag{1.1}$$

$$RT = \frac{RTA}{A_T} \tag{1.2}$$

where $A_T$ is the total area of the device defined by

$$A_T = \left(W + 2 \cdot FMIN \cdot 10^{-6}\right) \cdot \left(L + 4 \cdot FMIN \cdot 10^{-6}\right) \tag{1.3}$$

Note that the total thermal area is not simply equal to the gate area (W multiplied by L), but includes the source/drain contact regions, as well as any overlap around the gate. STAG v2.5 employs an empirical scheme often used by circuit designers to provide an estimate of total device size, based on the minimum feature size of the process technology, FMIN. These additional contributions from FMIN are important when calculating thermal parameters for devices which approach the minimum feature size in either dimension. The units of FMIN are microns ($\mu$m); the factors of $10^{-6}$ are included because W and L are given in metres (m). FMIN defaults to zero if not defined in the model netlist.

Tests performed on short/narrow channel devices have shown that leaving FMIN set to zero results in a serious overestimation of RT, and a corresponding underestimation of CT. If process layout data is available, then an optimal value of FMIN may be deduced which may differ from the actual minimum feature size. If, however, no process data is available for a particular technology, it is *strongly recommended* that FMIN be set equal to the value (in microns) of the process minimum feature width, simply to provide a reasonable order of magnitude estimate for the self-heating, i.e. when simulating a 0.35$\mu$m process, set FMIN to 0.35. Since total device area is also important for calculating accurate default values for certain overlap capacitances in STAG v2.5, it is good practise to include a value for FMIN whenever a new netlist is created, irrespective of the self-heating model being used. It is always possible to override any default parameter value calculated from FMIN.

3. If neither RT/CT or RTA/CTA are specified by the user, STAG v2.5 will calculate default values, using a first-order physical model. The relations used are

$$CT = \rho_{si} \cdot c_{si} \cdot A_T \cdot TB \tag{1.4}$$

$$RT = \frac{TOB}{\kappa_{ox} \cdot A_T} \tag{1.5}$$

where $\rho_{si}$ is the density of silicon ($2330kgm^{-3}$), $c_{si}$ is the heat capacity per unit mass of silicon ($700JK^{-1}kg^{-1}$), and $\kappa_{ox}$ is the thermal conductivity of the silicon oxide ($1.4WK^{-1}m^{-1}$). TB and TOB are the model parameters specifying the silicon film thickness and back oxide thickness respectively.

**Advanced Self-Heating Model**

For more precise modelling of thermal self-heating behaviour, additional thermal nodes may be introduced, each one possessing an associated thermal resistance and capacitance element. Under this regime, RT and CT effectively become RT0 and CT0, with RT1-4 and CT1-4 then providing the facility to model up to four additional thermal nodes. The existence of each thermal node requires first that its associated resistance be set to a non-zero value, but also that all preceeding thermal resistances be non-zero. For example, setting RT2 to zero will not only disable the third thermal node, but will also preclude use of the fourth and fifth thermal nodes as well. Unlike the first-order thermal parameters RT and CT, RT1-4 and CT1-4 automatically default to zero. This arrangement means that the basic self-heating model, which is more appropriate for most circuit design work, is switched on by default, while the more specialised model needs to be specifically activated by the user.

The multiple node model is chiefly intended for detailed modelling of thermal characteristics, and is appropriate when multiple thermal time constants have been extracted experimentally and need to be incorporated into simulations. In such instances, it will often be more appropriate to use extracted values to specify RT, RT1, RT2 etc, rather than rely on a scaling model. For this reason, no scaling model is provided for RT1-4 and CT1-4. The area scaling regime can still be applied to RT and CT (provided of course that RTA/CTA or the default values are used).

### Switching Off Self-Heating

To switch off self-heating for a single SOI device, simply set RT to zero. As discussed in the previous section, this will eliminate all the thermal nodes from that device, regardless of the settings of the other thermal parameters. To switch off self-heating for all SOI devices, set RTA to zero. Be aware that this will only work for devices for which RT is not set; because of the order of priorities for calculating RT, any device with a non-zero RT will ignore the RTA setting.

To switch off dynamic self-heating effects only, for a single device, set CT to zero, whilst leaving RT set. To do this for all devices, set CTA to zero, whilst leaving RTA set.

## 1.2.2 Threshold Voltage Modelling

STAG is a surface potential based model, and requires an accurate estimate of the flat band voltage in order to predict the onset of inversion. Although this value can be entered directly using the parameter VFBF, it is more usual to provide a measured value of threshold voltage and have the model calculate the flat band voltage using the standard MOSFET relation

$$VFBF = VT0 - \psi_{si} - \gamma\sqrt{\psi_{si}} \tag{1.6}$$

$$\psi_{si} = 2\phi_F \tag{1.7}$$

STAG v2.5 includes this standard relation, but since the above equation is not intended for measured values of threshold voltage, it is often necessary to optimise the value of VT0 in order to obtain a good fit with measured data. Therefore, STAG v2.5 also includes a new relation which is intended to provide a more precise theoretical relationship between the flat band voltage and measured values of threshold voltage

$$VFBF = VTEX - \psi_{si} - \gamma\sqrt{\psi_{si} + \phi_t \exp\left(\frac{DELTA0 \cdot \phi_F}{\phi_t}\right)} \tag{1.8}$$

$$\psi_{si} = (2 + DELTA0) \cdot \phi_F + 0.5VDEX \tag{1.9}$$

where VTEX is the extracted threshold voltage, VDEX is the drain voltage at which the measurement was taken, and DELTA0 is a surface potential factor which compensates for the difference between measured values of threshold voltage and the standard surface potential definition assumed in (1.6).

DELTA0 can be expected to vary with technology and extraction technique. Evaluation of the new model has shown that when VTEX is obtained using the linear extrapolation method, the typical range for DELTA0 is 0.05 to 0.1. Values outside this range are possible where a given technology exhibits particularly high or low vertical mobility degradation (or series resistance, if this is not accounted for in the measurement).

Note that adjustment of DELTA0 is not intended to compensate for other factors that might affect threshold voltage. One example are threshold shifts in short or narrow-channel devices, which are accounted for in STAG by parameters DELTAL and DELTAW. Such influences must be properly accounted for before optimising DELTA0.

### 1.2.3 Source and Drain Series Resistance

STAG models the effect of source and drain series resistance using two lumped resistances, RS and RD. It is possible to specify these parameters using three regimes, which are described below in order of priority.

1. By directly specifying RS and RD, the user overrides all other priorities.

2. The user can define the series resistance in terms of sheet resistance.

$$RS = NRS \cdot RSH \tag{1.10}$$

$$RD = NRD \cdot RSH \tag{1.11}$$

where RSH is the sheet resistance, and NRS/NRD are the number of squares associated with the source and drain (these are specified as instance parameters for each device).

3. The user can ensure that series resistances scale automatically with device width by using the source/drain series resistance scaling factors, RSW/RDW. We define RSW as the product of the source series resistance (ohms), and the width (in microns) of the device from which it was extracted. RDW is similarly obtained by multiplying RD and W for a single device. Note that device width is usually given in metres; the units of microns are only used here to calculate RSW and RDW. Once these values are in place, scaling can be performed for any device, using the following relations

$$RS = \frac{RSW}{W \cdot 10^{-6}} \tag{1.12}$$

$$RD = \frac{RDW}{W \cdot 10^{-6}} \tag{1.13}$$

### 1.2.4 Parasitic Bipolar Transistor

STAG v2.5 uses the same BJT current source expressions as STAG v2.1. These are repeated here for convenience

$$I_{BJTdb} = \alpha_{BJT} I_{bs\mathrm{diff}} \tag{1.14}$$

$$I_{BJTsb} = \alpha_{BJT} I_{bd\mathrm{diff}} \tag{1.15}$$

where $I_{bsdiff}$ and $I_{bddiff}$ are the diffusion currents, and $\alpha_{BJT}$ is defined as

$$\alpha_{BJT} = \frac{\beta_{BJT\mathrm{eff}}}{\beta_{BJT\mathrm{eff}} + 1} \tag{1.16}$$

where $\beta_{BJTeff}$ is the effective large signal current gain of the parasitic bipolar junction transistor. STAG v2.5 uses a new empirical expression to model the dependence of $\beta_{BJTeff}$ on device channel length.

$$\beta_{BJTeff} = \frac{BETABJT}{(L_{eff})^{BETAEXP}} \tag{1.17}$$

where BETAJBT and BETAEXP are model parameters. Note that $\beta_{BJTeff}$ is dimensionless; as a result, the units of BETAJBT will depend on the value chosen for BETAEXP. The default value of BETAEXP is 2, which gives the same inverse square relation as was used in STAG v2.1. For this case, the units of BETABJT are $m^2$, which is the default value given in Table 1.1 at the end of this user guide.

### 1.2.5 Intrinsic Body Charge Model

The previous version of STAG, v2.1, models the body charge by dividing it up between non-saturation charge $Q_{B1}$ and saturation charge $Q_{B2}$, as below:

$$Q_{B1} = W \int_0^{L'} q_b dy \tag{1.18}$$

$$Q_{B2} = 0 \tag{1.19}$$

where $q_b$ is the body charge density and L is the device channel length. The reason for setting $Q_{B2}$ to zero is due to the difficulty of deriving an expression for $q_b$ in the saturation region. Instead, it is intended that the intrinsic body capacitance associated with this region be lumped with the junction capacitance.

In STAG v2.5, a new model has been introduced to account for the intrinsic portion of the saturation body charge separately from the junction capacitance. We define $Q_{B2}$ as

$$Q_{B2} = W \int_0^{CSF \cdot l_d} q_b dy \tag{1.20}$$

where $l_d$ is the saturation region length, and CSF is an empirical charge sharing factor which expresses the fraction of the saturation region to which we associate intrinsic body charge (as opposed to charge associated with the drain-body pn junction). CSF is assigned a value between 0 and 1; the default value is 0.5, since setting it to zero was shown to often result in non-physical behaviour. Rather than modify the junction capacitance, it is recommended that they be left at their default values where possible, and CSF adjusted to provide the correct fit.

### 1.2.6 Source and Drain Junction Depletion Capacitance

The model priorities for calculating drain-body and source-body junction depletion capacitances, CBD and CBS are given below:

1. By directly specifying values for CBD and CBS in the model netlist, the user overrides all other priorities.

2. The user can provide a value for CJ, the junction capacitance per unit area of junction sidewall. STAG will then calculate CBD and CBS from CJ

$$CBD = \frac{CJ \cdot W \cdot TB}{\left(1 - \frac{Vdb}{PB}\right)^M} \quad if\ V_{db} < FC \cdot PB \tag{1.21}$$

$$CBD = \frac{CJ \cdot W \cdot TB}{(1 - FC)^{(1+M)}} \left[1 - FC\,(1 + M) + \frac{V_{db}}{PB} M\right] \quad if\ V_{db} \geq FC \cdot PB \tag{1.22}$$

where FC, PB, and M are empirical model parameters, and $V_{db}$ is the drain voltage. TB is the silicon film thickness. A similar expression can be obtained for the source-body junction capacitance, by replacing $V_{db}$ with $V_{sb}$.

3. If neither CBD/CBS or CJ are provided, then STAG v2.5 will calculate a default value for CJ using the following relation:

$$CJ = \sqrt{\frac{\varepsilon_0 \varepsilon_{si} q}{2\phi_{bi}} \left( \frac{NSUB \cdot NPLUS}{NSUB + NPLUS} \right)} \tag{1.23}$$

where NSUB is the silicon film doping concentration, NPLUS is the source/drain region doping concentration (defaults to $10^{20} cm^{-3}$), and $\phi_{bi}$ is the thermal equilibrium voltage across the pn junction, defined as

$$\phi_{bi} = \phi_t \ln \left( \frac{NSUB \cdot NPLUS}{n_i^2} \right) \tag{1.24}$$

If the need arises to switch off the junction depletion capacitances (for instance to test the intrinsic capacitance model without interference from other capacitance contributions) then CJ can be set to zero in the model netlist.

### 1.2.7 Overlap Capacitances

Most overlap capacitances in STAG v2.5 default to zero unless the appropriate overlap capacitance factor is set. In the case of the back gate-drain and back gate-source overlap capacitances, we can calculate default values based on the device geometry if the back gate overlap capacitance factors are not provided. The following relation is used:

$$C_{gbdo} = \frac{\epsilon_0 \cdot \epsilon_{ox} \cdot (2 \cdot FMIN \cdot 10^{-6}) \cdot W}{TOB} \tag{1.25}$$

The units of FMIN are microns ($\mu$m), so a factor of $10^{-6}$ is needed to convert to metres.

## 1.3 Element card

An element card specifying an SOI MOSFET modelled with STAG in SPICE 3f5 has the following format:

```
Axxxx ND NGf NS NGb NB NT MNAME
+ <L=VAL> <W=VAL> <NRD=VAL> <NRS=VAL>
+ <RT=VAL> <RT1=VAL> <RT2=VAL> <RT3=VAL> <RT4=VAL>
+ <CT=VAL> <CT1=VAL> <CT2=VAL> <CT3=VAL> <CT4=VAL>
+ <IC=VDS,VGfS,VGbS,VBS> <OFF> <TEMP=T>
```

Very few letters of the alphabet remained unused by the normal SPICE program. As the letter S is used by a SOS model developed previously at Southampton University, it was decided to use the letter A to denote an SOI device. ND, NGf, NS, NGb and NB are the drain, front gate, source, back gate (substrate) and body contact respectively. NT is the thermal node representing the local MOSFET temperature rise, and can be used to construct a thermal netlist. Both NT and NB can be left floating by specifying dummy node names. SPICE3 allows the node names to be alphanumeric, so a useful convention may be to have thermal nodes called T1, T2, ... etc.

MNAME is the model name. L and W are the nominal length and width of the device respectively, given in metres. If L or W are not given, default values are used. NRD and NRS are the equivalent number of squares of the drain and source respectively and both default to 1. These are used with RSH in the **.MODEL** card to obtain the drain and source resistances. RT and CT are the (first order) thermal resistance and thermal capacitance of the device. If RT is not specified, simulations are carried out without self-heating. The optional IC and OFF statements are for use in transient analyses to allow the user to set the device initial conditions. The optional TEMP value allows the user to specify the ambient temperature of the device and overrides the temperature specification in the .OPTION control line.

## 1.4 Model card

A model card specifying the STAG v2.1 parameters in SPICE 3f5 has the following general format:
After the model name MNAME, the parameter NSOI or PSOI must be specified to indicate that the model is used for either an n-channel or p-channel SOI MOSFET respectively. LEVEL should be set to 3 to select the surface potential based partially depleted SOI MOSFET model. Levels 1 and 2 refer to relatively simple current based fully and partially depleted SOI MOSFET models. These models are intended for internal use only and are not supported. After this comes a list of model parameters which are assigned values via the format

*parameter_name* `= VAL`.

Table 1.1 on the following page gives the names, descriptions and default values for all parameters of version 2.1 of the STAG SOI MOSFET model.

| Name | Parameter | Units | Default |
|---|---|---|---|
| LEVEL | model index | - | 3 |
| TNOM | parameter measurement temperature | °C | 27 |
| TOF | front oxide thickness ($t_{of}$) | m | required |
| TOB | back oxide thickness ($t_{ob}$) | m | required |
| TB | silicon film thickness ($t_b$) | m | required |
| TPG | type of gate material: | - | 1 |
| | 1 opposite to substrate | | |
| | -1 same as substrate | | |
| | 0 aluminium gate | | |
| NQFF | front fixed charge density | $cm^{-2}$ | 0 |
| NSSF | front fast surface state density | $cm^{-2}eV^{-1}$ | 0 |
| NSUB | silicon film doping concentration ($N_A$) | $cm^{-3}$ | required |
| PHI | surface potential ($\phi = 2\phi_F$) | V | derived † |
| CHIPHI | surface potential temperature dependence | V/K | 0 |
| GAMMA | body factor | $V^{\frac{1}{2}}$ | derived † |
| LD | lateral diffusion | m | 0 |
| VT0 | zero bias threshold voltage ($V_{th0}$) | V | derived † |
| VTEX | measured threshold voltage | V | 0 |
| VDEX | measurement drain voltage | V | 0 |
| DELTA0 | surface potential factor | – | 0 |
| VFBF | flatband voltage | V | derived † |
| DELTAL | threshold roll-off with channel length | m | 0 |
| DELTAW | threshold roll-up with channel width | m | 0 |
| SIGMA | drain induced barrier lowering | m | 0 |
| CHIFB | flatband voltage temperature dependence | V/K | 0 |
| U0 | zero field surface mobility ($\mu_0$) | $cm^2/Vs$ | 600 |
| THETA | vertical field mobility degradation ($\theta$) | $V^{-1}$ | 0 |
| VSAT | carrier saturation velocity | cm/s | 0 †† |
| K | mobility temperature exponent | – | 1.5 |
| KP | transconductance parameter | $A/V^2$ | derived † |
| LAMBDA | channel length modulation factor ($\lambda$) | m/V | 0 |
| VP | fitting parameter (second CLM model) | V | 0 ††† |
| LX | effective pinch-off region length (second CLM model) | m | 0 ††† |

**Table 1.1:** *Names, descriptions and default values for all parameters of version 2.1 of the STAG partially depleted SOI MOSFET model.* *Continued on next page ...*

| Name | Parameter | Units | Default |
|---|---|---|---|
| RSH | drain and source diffusion sheet resistance | Ω/sq | 0 |
| RD | drain series resistance | Ω | derived ‡ |
| RS | source series resistance | Ω | derived ‡ |
| RDW | scalable drain series resistance factor | Ω.$\mu$m | 0 |
| RSW | scalable source series resistance factor | Ω.$\mu$m | 0 |
| JS | junction saturation current density per metre width | A/m | 1E-10 |
| ETAD | junction ideality coefficient | – | 1 |
| JS1 | second junction saturation current density per metre width | A/m | 0 |
| ETAD1 | second junction ideality coefficient | – | 1 |
| IS | junction saturation current | A | derived ‡‡ |
| IS1 | second junction saturation current | A | derived ‡‡ |
| CHID | temperature coefficient of IS | eV.K/J | $E_g/k$ |
| CHID1 | temperature coefficient of IS1 | eV.K/J | $E_g/k$ |
| DVT | switch for $\phi_t$ temperature dependence (diodes only) | – | 1 |
| CSF | saturation body charge sharing factor | – | 0.5 |
| NPLUS | drain/source region doping concentration | $\mathrm{cm}^{-3}$ | 1E20 |
| CJ | zero-bias junction capacitance per square metre of (sidewall) junction area | $\mathrm{F/m}^2$ | 0 |
| CBD | zero bias body-drain junction capacitance | F | derived ‡‡‡ |
| CBS | zero bias body-source junction capacitance | F | derived ‡‡‡ |
| PB | junction potential | V | 0.8 |
| MJ | junction grading coefficient | – | 0.5 |
| FC | junction forward bias coefficient | – | 0.5 |
| RTA | scalable thermal resistance factor | $\mathrm{m}^2.K/\mathrm{W}$ | 0 |
| CTA | scalable thermal capacitance factor | $\mathrm{J/m}^2.\mathrm{K}$ | 0 |
| ALPHA0 | first impact ionisation constant | 1/cm | 0 |
| BETA0 | second impact ionisation constant | V/cm | 1.92E6 |
| CHIBETA | temperature coefficient of BETA0 | V/cm.K | 0 |
| ETA | effective field factor | – | 1 |
| LM | effective ionisation length | m | 0 |
| LM1 | LM variation with gate voltage | m/V | 0 |
| LM2 | LM variation with gate voltage squared | $\mathrm{m/V}^2$ | 0 |

*continued on next page ...*

| Name | Parameter | Units | Default |
|---|---|---|---|
| BETABJT | parasitic bipolar current gain parameter | $m^2$ (default) ‡‡‡‡ | 0 |
| BETAEXP | parasitic bipolar current gain exponent | – | 2 |
| TAUF | bipolar forward transit time | s | 0 |
| TAUR | bipolar reverse transit time | s | 0 |
| NLEV | 1/f noise model level:<br>0 $1/f\ (\mathrm{KF}\,.\,I_D^{\mathrm{AF}})/(L^2\,.\,C_{of})$<br>1 $1/f\ (\mathrm{KF}\,.\,I_D^{\mathrm{AF}})/(W\,.\,L\,.\,C_{of})$<br>2 $1/f^{\mathrm{AF}}\ (\mathrm{KF}\,.\,g_m^2)/(W\,.\,L\,.\,C_{of})$ | – | 0 |
| AF | 1/f noise exponent | – | 1 |
| KF | 1/f noise coefficient | see NLEV | 0 |
| CGFSO | front gate-source overlap capacitance per metre channel width | F/m | 0 |
| CGFDO | front gate-drain overlap capacitance per metre channel width | F/m | 0 |
| CGFBO | front gate-bulk overlap capacitance per metre channel length | F/m | 0 |
| CGBSO | back gate-source overlap capacitance per metre channel width | F/m | 0 |
| CGBDO | back gate-drain overlap capacitance per metre channel width | F/m | 0 |
| CGB_BO | back gate-bulk overlap capacitance per metre channel length | F/m | 0 |
| FMIN | process minimum feature size | $\mu$m | 0 |

† When not given, an estimate is derived from other model parameters.

†† A value of 0 is a switch to exclude velocity saturation effects.

††† To select the second channel length modulation model, specify VP and LX *and do not specify* LAMBDA.

‡ Calculated from the sheet resistance RSH, and NRS or NRD.

‡‡ Calculated from the current density JS or JS1, and the channel width.

‡‡‡ Calculated from the capacitance per unit area CJ, the channel width and the film thickness.

‡‡‡‡ Units of BETABJT are dependent on value chosen for BETAEXP ($m^2$ corresponds to default BETAEXP value of 2).